

**IN THE UNITED STATES DISTRICT COURT  
FOR THE DISTRICT OF DELAWARE**

<p>LG DISPLAY CO., LTD.,</p> <p style="text-align: center;">v.</p> <p>CHI MEI OPTOELECTRONICS CORPORATION, et al.,</p>	<p style="text-align: center;">Plaintiff,</p> <p style="text-align: center;">Defendants.</p>	<p>Civil Action No. 06-726 (JJF) Civil Action No. 07-357 (JJF)</p> <p style="text-align: center;"><b>CONSOLIDATED CASES</b></p>
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**AMENDED JOINT CLAIM CONSTRUCTION CHARTS**

Pursuant to the Court's May 19, 2008 Stipulation and Order Modifying the Scheduling Order (D.I. 208), LG Display Co., Ltd. and LG Display America, Inc. ("LG Display"), Chi Mei Optoelectronics Corporation and Chi Mei Optoelectronics USA, Inc. ("CMO"), and AU Optronics Corporation and AU Optronics Corporation America ("AUO") submit their Joint Claim Construction Charts as follows:

**I. Patents asserted by LG Display:**

U.S. Patent No. 4,624,737	Exhibit A
U.S. Patent No. 5,019,002	Exhibit B
U.S. Patent No. 5,825,449	Exhibit C
U.S. Patent No. 6,664,569	Exhibit D
U.S. Patent No. 6,803,984	Exhibit E
U.S. Patent No. 5,905,274	Exhibit F
U.S. Patent No. 6,815,321	Exhibit G
U.S. Patent No. 7,176,489	Exhibit H
U.S. Patent No. 7,218,374	Exhibit I

**II. Patents asserted by AUO:**

U.S. Patent No. 5,748,266	Exhibit J
U.S. Patent No. 6,689,629	Exhibit K
U.S. Patent No. 6,734,944	Exhibit L
U.S. Patent No. 6,778,160	Exhibit M
U.S. Patent No. 6,976,781	Exhibit N

U.S. Patent No.7,090,506	Exhibit O
U.S. Patent No. 7,101,069	Exhibit P
U.S. Patent No. 7,125,157	Exhibit Q

**III. Patents asserted by CMO:**

U.S. Patent No. 5,619,352	Exhibit R
U.S. Patent No. 6,008,786	Exhibit S
U.S. Patent No. 6,013,923	Exhibit T
U.S. Patent No. 6,134,092	Exhibit U
U.S. Patent No. 6,734,926	Exhibit V
U.S. Patent No. 7,280,179	Exhibit W

Each party has listed what it contends is intrinsic evidence to support its contentions. All parties reserve the right to contest whether any such evidence is intrinsic or extrinsic.

August 6, 2008

/s/ Richard D. Kirk

OF COUNSEL:

Gaspare J. Bono  
 Song K. Jung  
 R. Tyler Goodwyn, IV  
 Lora A. Brzezynski  
 MCKENNA LONG & ALDRIDGE LLP  
 1900 K Street, N.W.  
 Washington, D.C. 20006  
 (202) 496-7500

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Richard D. Kirk (#0922)  
 Ashley B. Stitzer (#3891)  
 THE BAYARD FIRM  
 222 Delaware Avenue, 9th Floor  
 P.O. Box 25130  
 Wilmington, DE 19899-5130  
 (302) 655-5000  
 rkirk@bayardfirm.com  
*Attorneys for LG Display Co., Ltd. and LG  
 Display America, Inc.*

OF COUNSEL:

Jonathan S. Kagan  
 Alexander C.D. Giza  
 Adam Hoffman  
 IRELL & MANELLA LLP  
 1800 Avenue of the Stars, Suite 900  
 Los Angeles, California 90067-4276  
 (310) 277-1010

---

Philip A. Rovner (#3215)  
 POTTER ANDERSON & CORROON LLP  
 Hercules Plaza  
 P.O. Box 951  
 Wilmington, DE 19899  
 (302) 984-6000  
 provner@potteranderson.com  
*Attorneys for Chi Mei Optoelectronics  
 Corporation and Chi Mei Optoelectronics USA,  
 Inc.*

OF COUNSEL:

Vincent K. Yip  
Peter J. Wied  
Terry Garnett  
Katherine Murray  
PAUL HASTINGS JANOFSKY & WALKER LLP  
515 South Flower Street, 25th Floor  
Los Angeles, CA 90071  
(213) 683-6000

M. Craig Tyler  
Brian D. Range  
WILSON SONSINI GOODRICH & ROSATI  
8911 Capital of Texas Highway North  
Westech 360, Suite 3350  
Austin, TX 78759-8497  
(512) 338-5400

Ron E. Shulman  
Julie M. Holloway  
WILSON SONSINI GOODRICH & ROSATI  
650 Page Mill Road  
Palo Alto, CA 94304-1050

/s/ Karen L. Pascale

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John W. Shaw (#3362)  
Karen L. Pascale (#2903)  
YOUNG CONAWAY STARGATT & TAYLOR LLP  
The Brandywine Building  
1000 West Street, 17th Floor  
P.O. Box 391  
Wilmington, DE 19899-0391  
(301) 571-6600  
kpascale@ycst.com

*Attorneys for AU Optronics Corporation and AU Optronics Corporation America*

# **EXHIBIT A**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT A**  
**LG DISPLAY USP 4,624,737**

<b>Claim Terms</b>	<b>Des.</b>	<b>Agreed Constructions</b>
insulating substrate	C	The material (such as glass, quartz, ceramic, insulator-coated silicon or insulator coated metal) upon which the transistor is fabricated to provide mechanical support and electrical insulation.

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
a process for producing a thin-film transistor	C	<p>a method for manufacturing thin-film transistors such as for a liquid crystal display</p> <p><u>Intrinsic Support</u>            1:6-29; 1:56-58; 1:61-68;            2:1-2; 2:8-68; 3:1-62; 4:1-23; Figs 1a-3d.</p>	plain meaning in light of the construction below for “thin-film” transistor	Plain meaning.

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
thin-film transistor	C	<p>A three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.</p> <p><u>Intrinsic Support</u>  1:6-29; 1:56-58; 1:61-68;  2:1-2; 2:8-68; 3:1-62; 4:1-23; Figs 1a-3d.</p>	<p>A three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semi-conductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than in a single crystal silicon wafer.</p> <p><u>Intrinsic Support</u>  1:8-31; 1:47-53; 4:3-12 see also 5/5/05 Order re Claim Construction, Case No. 02-6775, at 13; Second Revised Joint Claim Construction Statement, Case No. 02-6775, at 89-93</p>	<p>Plain meaning.</p> <p>Alternate: A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.</p> <p><u>Intrinsic Support</u>  E.g., Figs. 2-3; 1:8-29; 1:56-58; 2:8-4:2</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
forming a gate electrode on an insulating substrate	C	<p>giving form or shape to a patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode that is above and supported by or in contact with material (such as glass, quartz, ceramic, insulator-coated silicon or insulator coated metal) upon which the transistor is fabricated to provide mechanical support and electrical insulation</p> <p><u>Intrinsic Support</u></p> <p>1:14-21; 2:8-24; 3:21-39; Figs 1a-3d.</p>	plain meaning	<p>Producing a gate electrode above, supported by, and in contact with an insulating substrate</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2: 8-16; 3:23-28</p>
forming ... on	C	<p>giving form or shape to...above and supported by or in contact with</p> <p><u>Intrinsic Support</u></p> <p>1:14-17; 2:8-17; 3:21-39; Figs 1a, 2a, 3a.</p>	plain meaning	<p>Producing . . . above, supported by, and in contact with</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2: 8-16; 3:23-35</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film	C	<p>the formation of the gate insulating film, the high-resistivity semiconductor film and conducting film (without intervening films) above and supported by or in contact with (i) the patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode and (ii) the material (such as glass, quartz, ceramic, insulator-coated silicon or insulator coated metal) upon which the transistor is fabricated to provide mechanical support and electrical insulation.</p> <p><u>Intrinsic support</u></p> <p>1:14-53; 1:55-58; 2:8-45; 3:21-35; 3:54-62; 4:3-24; Figs 2a-3d; Abstract.</p>	<p>construe the term:  "depositing on said gate electrode and substrate"  as:  depositing above and in contact with the gate electrode and the insulating substrate</p> <p><u>Intrinsic Support</u></p> <p>1:17-38; 3:28-35; 3:53-4:2; 4:17-23; Figs. 1a-1d, 2b, 3b (e.g., elements 1, 2, 3)</p>	<p>Precipitating a gate insulating film, a high resistivity semiconductor film and a conductive film on the gate electrode and the substrate without intervening films in between.</p> <p><u>Intrinsic Support</u></p> <p>E.g., Abstract; Figs. 2-3; 1:32-46; 2:17-53; 3:22-4:12</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
continuously depositing	L C A	<p>the formation of the gate insulating film, the high-resistivity semiconductor film and conducting film without intervening films</p> <p><u>Intrinsic Support</u></p> <p>1:17-21; 2:17-45; 3:28-35; 3:54-62; 4:1-13; Abstract; Figs 2b and 3b.</p>	<p>the formation of the gate insulating film, the high-resistivity semiconductor film and conducting film without intervening films</p> <p><u>Intrinsic Support</u></p> <p>1:17-38; 3:28-35; 3:53-4:2; 4:17-23; Figs. 1a-1d, 2b, 3b (e.g., elements 3, 4, 20 and 30) see also 5/5/05 Order re Claim Construction, Case No. 02-6775, at 8-9; Second Revised Joint Claim Construction Statement, Case No. 02-6775, at 95-101.</p>	<p>Precipitating... without intervening films</p> <p><u>Intrinsic Support</u></p> <p>E.g., Abstract; Figs. 2-3; 1:32-46; 2: 17-53; 3:22-4:12</p>
depositing on	C	<p>the formation of the gate insulating film, the high-resistivity semiconductor film and conducting film above and supported by or in contact with</p> <p><u>Intrinsic Support</u></p> <p>1:14-21; 2:8-45; 3:28-35; 3:54-62; 4:1-13; Abstract; Figs 2b and 3b.</p>	<p>this term should be construed as part of the larger term “depositing on said gate electrode and substrate”</p>	<p>precipitating above, supported by and in contact with</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:17-53; 3:22-4:12</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
depositing	A	<p>the formation of the gate insulating film, the high-resistivity semiconductor film and conducting film</p> <p><u>Intrinsic Support</u></p> <p>1:17-21; 2:17-45; 3:28-35; 3:54-62; 4:1-13; Abstract; Figs 2b and 3b.</p>	plain meaning	<p>Precipitating</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:17-53; 3:22 - 4:12</p>
gate insulating film	C	<p>a thickness of non-conductive material (such as SiNx) that has a high electrical resistance and insulates the transistor gate from the semiconductor.</p> <p><u>Intrinsic Support</u></p> <p>1:12-21, 2:18-38; 3:28-35; Abstract; Figs. 1b-1d, 2b-2e, and 3b-3d.</p>	<p>a thickness of material (such as SiNx, SiOx, or a multi-layer film made of such materials) with a high electrical resistance, spanning the region from the gate electrode to the high resistivity semiconductor layer, for insulating the gate electrode from the channel</p> <p><u>Intrinsic Support</u></p> <p>1:17-21; 4:17-23; 1:32-40; 4:47-53 (Claim 2); 4:26-46 (Claim 1); 3:53-4:2; Figs 2a-2e, 3</p>	<p>Plain meaning</p> <p>or</p> <p>Insulating film formed over the gate region</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:17-53; 3:22-4:12</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
high-resistivity semiconductor film	C	<p>a thickness of semiconductor material (such as amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline amorphous silicon) that has a higher resistance to current flow relative to the low-resistivity semiconductor film.</p> <p><u>Intrinsic Support</u></p> <p>1:8-29; 1:32-49; 2:17-32; 2:38-43; 2:54-60; 3:7-10; 3:16-21; 3:28-41; 4:48-62; 4:1-23; Abstract; Figs. 1b-1d, 2b-2e, and 3b-3d.</p>	<p>a thickness of semiconductor material (such as amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline amorphous silicon) that has a high resistance to current flow and acts as the channel of the transistor</p> <p><u>Intrinsic Support</u></p> <p>1:32-51; 2:8-10; 2:38-43; 2:60-3:4; Figs. 2b-2e, 3b-3d (e.g., element 4)</p>	<p>Plain meaning</p> <p>or</p> <p>Semiconductor having the property of high resistivity</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:17-53; 3:22-4:12</p>
conducting film	C	<p>a thickness of electrically conductive material</p> <p><u>Intrinsic Support</u></p> <p>1:25-29; 1:32-51; 2:10-36; 2:43-68; 3:1-10; 3:28-35; 3:48-62; 4:1-23; Abstract; Figs. 2b-2e and 3b-3d.</p>	<p>a thickness of electrically conductive material that lies adjacent to the channel layer</p> <p><u>Intrinsic Support</u></p> <p>2:17-21; 2:46-3:10; 3:53-4:2; Figs. 2b-2e, 3b-3d (e.g., elements 20, 30)</p>	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:17-53; 3:22-4:12</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
a conducting film containing at least a low-resistivity semiconductor film	L C A	<p>the conducting film is composed of a low-resistivity semiconductor film and possibly other conductive films</p> <p><u>Intrinsic Support</u></p> <p>1:18-36; 1:43-57; 2:17-37; 3:28-41; 3:48-62; 4:1-13, Abstract, Figs.2b-2e and 3b-3d.</p>	<p>plain meaning</p> <p>the terms "conducting film" and "low-resistivity semiconductor film" should be construed separately from this term</p>	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2: 17-53; 3:22-4:12</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
low-resistivity semiconductor film	C	<p>a thickness of semiconductor material (such as low-resistivity amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline amorphous silicon which contains phosphorous or other impurities to enhance the conductivity of the film) that has a lower resistance to current flow relative to the high-resistivity semiconductor film.</p> <p><u>Intrinsic Support</u></p> <p>1:25-29; 1:32-51; 2:17-50; 2:54-68; 3:1-10; 3:28-41; 3:48-62; 5:1-23; Abstract; Figs. 1d, 2b-2e, 3b-3d.</p>	<p>a thickness of semiconductor material (such as amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline amorphous silicon) that has a low resistance to current flow</p> <p><u>Intrinsic Support</u></p> <p>1:32-51; 2:17-21; 2:38-44; 3:53-4:2; Figs. 2b-2e, 3b-3d (e.g., element 20)</p>	<p>Plain meaning</p> <p>Or</p> <p>semiconductor having the property of low resistivity</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2: 17-53; 3:22 - 4:12</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
without exposing them to an oxidizing atmosphere	C	<p>without exposing the gate insulating film, the high-resistivity semiconductor film, and the conducting film containing at least the low-resistivity semiconductor film to an atmosphere that would create a detectable amount of oxidation on a film.</p> <p><u>Intrinsic Support</u></p> <p>1:32-46; 1:47-53; 2:17-36; 3:28-35; 3:53-62; 4:1-12; Figs. 2b-2e, 3b-3d.</p>	<p>without permitting the gate insulating film, high-resistivity semiconductor film, low-resistivity semiconductor film, or conducting film to come into contact with an uncontrolled ambient atmosphere which contains oxidizing agents</p> <p><u>Intrinsic Support</u></p> <p>1:32-51; 2:17-53; 3:28-35; Figs. 2b-2e, 3b-3d</p>	<p>Without exposing them to an atmosphere containing an oxidizing agent</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; Abstract; 1:32-46; 2:17-53; 3:22-4:12</p>
them	C	<p>the gate insulating film, the high-resistivity semiconductor film, and the conducting film containing at least the low-resistivity semiconductor film.</p> <p><u>Intrinsic Support</u></p> <p>2:17-36; 3:28-35; 3:53-62; 4:1-12; Abstract; Figs. 2b-2e, 3b-3d.</p>	<p>the gate insulating film, the high-resistivity semiconductor film, and the conducting film containing at least the low-resistivity semiconductor film</p>	<p>Indefinite.</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:17-53; 3:22-4:12</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
oxidizing atmosphere	C	<p>an atmosphere that would create a detectable amount of oxidation on a film.</p> <p><u>Intrinsic Support</u></p> <p>1:21-51; 2:17-53; 3:28-35; 3:53-4:23; Figs. 2b-2e, 3b-3d; Abstract.</p>	<p>an uncontrolled ambient atmosphere which contains oxidizing agents</p> <p><u>Intrinsic Support</u></p> <p>1:32-51; 2:17-53; 3:28-35; Figs. 2b-2e, 3b-3d</p>	<p>Atmosphere containing an oxidizing agent</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; Abstract; 1:32-46; 2:17-53; 3:22-4:12</p>
selectively etched	C	<p>The removal of selected portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) in order to produce a desired pattern on the surface.</p> <p><u>Intrinsic Support</u></p> <p>1:14-21; 1:25-29; 1:32-35; 2:10-16; 2:54-66; 3:7-10; 3:28-41; 3:44-48; 4:3-9; Figs 1a-d; 2a-e; 3a-d.</p>	<p>plain meaning</p>	<p>Selectively removed or corroded by a chemical agent</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:54-60; 3:22-4:12</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
they are partly left as an island region on said gate electrode	L	<p>a portion of the high resistivity semiconductor film and conducting film has been etched around its perimeter into a region located over the gate electrode of a thin-film transistor</p> <p><u>Intrinsic Support</u></p> <p>1:14-17; 1:25-29; 2:7-16; 2:54-66; 3:22-; Figs. 2-3.</p>	plain meaning	<p>Indefinite</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:54-60; 3:22-4:12</p>
island region on said gate electrode	C	<p>a portion of the high resistivity semiconductor film and conducting film has been etched around its perimeter into a region located over the gate electrode of a thin-film transistor.</p> <p><u>Intrinsic Support</u></p> <p>1:14-17; 1:25-29; 2:7-16; 2:54-66; 3:22-; Figs. 2-3.</p>	plain meaning	<p>Isolated region above, supported by, and in contact with the gate electrode</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:54-60; 3:22-4:12</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
gate electrode	C A	<p>a patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>1:14-18; 2:7-16; 3:33-29; Figs 1a-3d.</p>	<p>a patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>see 5/5/05 Order re Claim Construction, Case No. 02-6775, at 7-8; Second Revised Joint Claim Construction Statement, Case No. 02-6775 at 93-95</p>	<p>A patterned, electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:8-16; 3:23-28</p>
a fourth step for selectively forming a source electrode and drain electrode	C A	<p>forming a source electrode and drain electrode in selected regions only</p> <p><u>Intrinsic Support</u></p> <p>1:21-29; 1:32-51; 2:17-68; 3:1-14; 3:28-62; 4:1-12; Abstract; Figs. 1d, 2d-2e, 3c-3d.</p>	plain meaning	<p>Step-plus function element.</p> <p>Function is "selectively forming a source electrode and drain electrode"</p> <p>Step is disclosed: E.g., Figs. 2-3; 2:60-3:10; 3 :22-4:12</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
selectively forming	C	<p>forming in selected regions only</p> <p><u>Intrinsic Support</u></p> <p>1:14-17; 1:25-29; 2:10-36; 2:60-68; 3:1-10; 3:24-52; 4:3-9; Abstract; Figs. 1a-1d, 2a-2e, 3a-3d.</p>	<p>plain meaning</p>	<p>Selectively producing</p> <p><u>Intrinsic support</u></p> <p>E.g., Figs. 2-3; 2:60-3:10; 3:22-4:12</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
source electrode	C A	a patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.	construe term:  "a source electrode and a drain electrode"  as:  Patterned, electrically conductive material formed over the source region and drain region, respectively, of a transistor. Current flows through the channel between the source electrode and the drain electrode of the transistor under control of the gate electrode of the transistor.	A patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
drain electrode	C A	a patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source and drain electrode under the control of the gate electrode.  <u>Intrinsic Support</u>  1:21-29; 1:32-51; 2:17-68; 3:1-14; 3:28-62; 4:1-12; Abstract; Figs. 1d, 2d-2e, 3c-3d.	this term should be construed as part of the larger term “a source electrode and a drain electrode”	A patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.  <u>Intrinsic Support</u>  E.g., Abstract; 1:17-29; 2:60-3:10; 3:36-41
contacting a part of the surface of said island region	L C A	touching a part of the surface of the island region  <u>Intrinsic Support</u>  2:54-3:10; 3:53-62; 4:1-2; Figs 2d-2e; 3c-3d.	Touching a part of the surface of the island region  <u>Intrinsic Support</u>  2:60-66; 3:4-7; 3:36-41 Figs. 2d-2e, 3c-3d	Plain meaning  <u>Intrinsic Support</u>  E.g., Figs. 2-3; 2:60-3:10; 3:22-4:12

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask	A	<p>a fifth step for removing selected regions only of the conducting film on the island region not covered by the source electrode, drain electrode or mask wherein the source electrode and drain electrode serve as at least a part of the pattern above a surface from which material is to be selectively removed; the pattern is made of material that is resistive to the removal technique relative to the material to be removed</p> <p><u>Intrinsic Support</u></p> <p>1:14-54; 2:10-14; 2:54-68; 3:1-16; 3:24-52; Abstract; Figs 1a-1d, 2a-2e, 3a-3d.</p>	<p>eliminating all the conducting film in the space between the edges of the source and drain electrodes</p> <p><u>Intrinsic Support</u></p> <p>1:32-51; 2:60-66; 3:8-10; 3:36-41; 3:59-4:6; Figs. 2c-2e, 3b-3d</p>	<p>a fifth step for using the source and drain electrodes to partially define the boundary for the removal of the conducting film exposed on the island region.</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:60-3:10; 3:22-4:12</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
selectively removing said conducting film exposed on said island region	C	<p>removing selected regions only of the conducting film on the island region not covered by the source electrode, drain electrode or mask</p> <p><u>Intrinsic Support</u></p> <p>1:14-54; 2:10-14; 2:54-68; 3:1-16; 3:24-52; Abstract; Figs 1a-1d, 2a-2e, 3a-3d.</p>	<p>eliminating all the conducting film in the space between the edges of the source and drain electrodes</p> <p><u>Intrinsic Support</u></p> <p>1:8-31; 1:32-51; 2:60-66; 3:8-10; 3:36-41; 3:59-4:6; Figs. 1b-1d, 2c-2e, 3b-3d</p>	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:60-3:10; 3:22-4:12</p>
selectively removing	C	<p>removing selected regions only</p> <p><u>Intrinsic Support</u></p> <p>1:14-29; 2:10-14; 2:54-68; 3:1-16; 3:24-52; Abstract; Figs 1a-1d, 2a-2e, 3a-3d.</p>	<p>this term should be construed as part of the larger term, “selectively removing said conducting film exposed on said island region.”</p>	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:60-3:10; 3:22-4:12</p>
said conducting film exposed on said island region	A	<p>the conducting film on the island region that is not covered by the source electrode, drain electrode or mask</p> <p><u>Intrinsic Support</u></p> <p>1:14-54; 2:10-14; 2:54-68; 3:1-16; 3:24-52; Abstract; Figs 1a-1d, 2a-2e, 3a-3d.</p>	<p>Plain meaning</p>	<p>the conducting film on top of the island region exposed to the atmosphere</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:60-3:10; 3:22-4:12</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
said source and drain electrodes serving as at least a part of the mask	C A	<p>the source and drain electrodes serving as at least a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of material that is resistive to the removal technique relative to the material to be removed</p> <p><u>Intrinsic Support</u></p> <p>1:14-54; 2:10-14; 2:54-68; 3:1-16; 3:24-52; Abstract; Figs. 1a-1d, 2a-2e, 3a-3d.</p>	<p>the source and drain electrodes are part of the pattern on the top surface that protects underlying layer from being removed while allowing the portion of the layer exposed between the source and drain electrodes to be removed</p> <p><u>Intrinsic Support</u></p> <p>1:8-31; 1:32-51; 2:60-66; 3:8-10; 3:36-41; 3:59-4:6; Figs. 1b-1d, 2c-2e, 3b-3d</p>	<p>Using the source and drain electrodes to partially define the boundary for the removal or formation of the conductive film.</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:60-3:10; 3:22-4:12</p>
serving as at least a part of the mask	L	<p>serving as at least a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of material that is resistive to the removal technique relative to the material to be removed</p> <p><u>Intrinsic Support</u></p> <p>1:14-29; 2:10-14; 2:54-68; 3:1-16; 3:24-52; Abstract Figs. 1a-1d, 2a-2e, 3a-3d.</p>	<p>this term should be construed as part of the term "said source and drain electrodes serving as at least a part of the mask"</p> <p>see also construction of "mask" below</p> <p><u>Intrinsic Support</u></p> <p>1:8-31; 1:32-51; 2:60-66; 3:8-10; 3:36-41; 3:59-4:6; Figs. 1b-1d, 2c-2e, 3b-3d</p>	<p>using ... to partially define the boundary for the removal process</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:60-3:10; 3:22-4:12</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
at least a part of the mask	C	<p>at least a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of material that is resistive to the removal technique relative to the material to be removed.</p> <p><u>Intrinsic Support</u></p> <p>1:14-29; 2:10-14; 2:54-68; 3:1-16; 3:24-52; Abstract; Figs 1a-1d, 2a-2e, 3a-3d.</p>	<p>this term should be construed as part of the term “said source and drain electrodes serving as at least a part of the mask”</p>	<p>to partially define the boundary for the removal or formation process</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3, 2:60-3:10; 3:22-4:12</p>
a part of the mask	A	<p>a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of material that is resistive to the removal technique relative to the material to be removed.</p> <p><u>Intrinsic Support</u></p> <p>1:14-29; 2:10-14; 2:54-68; 3:1-16; 3:24-52; Abstract; Figs 1a-1d, 2a-2e, 3a-3d.</p>	<p>this term should be construed as part of the term “said source and drain electrodes serving as at least a part of the mask”</p>	<p>to partially define the boundary for the removal or formation process</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:60-3:10; 3:22-4:12</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
mask	A	<p>A pattern above a surface from which material is to be selectively removed. The pattern is made of material that is resistive to the removal technique relative to the material to be removed.</p> <p><u>Intrinsic Support</u></p> <p>1:14-29; 2:10-14; 2:54-68; 3:1-16; 3:24-52; Abstract; Figs 1a-1d, 2a-2e, 3a-3d.</p>	<p>A top surface pattern above one or more layers of material that will be selectively removed according to the shape of the mask. The mask is made of material that is resistive to the removal technique and defines by its edges the boundaries of the material selected for removal.</p> <p><u>Intrinsic Support</u></p> <p>1:8-31; 1:32-51; 2:60-66; 3:8-10; 3:36-41; 3:59-4:6; Figs. 1b-1d, 2c-2e, 3b-3d</p>	<p>A pattern to define the boundary for the removal or formation process</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 2:60-3:10; 3:22-4:12</p>
surface passivation film	C	<p>a thickness of material that provides protection such as electrical stability and chemical isolation</p> <p><u>Intrinsic Support</u></p> <p>1:29-31; 3:11-21; 3:44-48; Figs 2e, 3d.</p>	plain meaning	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-3; 3:11-21; 3:22-4:12</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
exposing a part of each of said source electrode, drain electrode and gate electrode	C A	removing portions of one or more layers to uncover a part of each of said source electrode, drain electrode and gate electrode  <u>Intrinsic Support</u>  1:6-31; 3:11-21; 3:36-52; Fig. 2e; 3d.	plain meaning	causing a part of the source electrode, drain electrode and gate electrode to be exposed to the atmosphere  <u>Intrinsic Support</u>  E.g., Figs. 2-3; 3:11-21; 3:22-4:12
exposing	A	removing portions of one or more layers to uncover  <u>Intrinsic Support</u>  1:6-31; 3:11-21; 3:36-52; Fig. 2e; 3d.		Uncovering  <u>Intrinsic Support</u>  E.g., Figs. 2-3; 3:11-21; 3:22-4:12

# **EXHIBIT B**

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**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
substrate	C	<p>the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support</p> <p><u>Intrinsic Support:</u> 1:34-38; 3:33-38; Figs. 1-7; Abstract.</p>	Plain meaning	<p>Plain meaning</p> <p><u>Intrinsic Support</u> E.g., Figs. 1-2; 37-38; 4:11-22; 4:67-5:2</p>
forming a pattern of pixels on said substrate	C	<p>depositing and etching a matrix of transparent electrically conductive material to form pixel electrodes above and supported by or in contact with the substrate</p> <p><u>Intrinsic Support</u> 1:38-2:6; 2:45-68; 3:3-21; 3:25-36; 3:47-59; 4:4-22, 4:42-45; 4:61-5:6, 5:24-32; 5:42-5:57; 6:46-6:50; 6:60-7:18; 7:47-7:60; 8:49-62; Figs. 1, 4-7; Figs. 1-6; Abstract.</p>	<p>forming a repeating configuration of redundant subpixels</p> <p><u>Intrinsic Support</u> 7:46-60; 4:58-60; 5:44-57; 6:19-25; 6:26-36; and figures referenced therein</p>	<p>Forming a pattern of pixels above, supported by and in contact with the substrate</p> <p><u>Intrinsic Support</u> E.g., Figs. 1, 2, 3, &amp; 6; 3:25-4:3; 5:2-6; 5:24-32</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
forming a plurality of row and column intersecting pixel activation lines	C	<p>depositing and etching electrically conductive material patterned in rows and columns that control pixels</p> <p><u>Intrinsic Support</u></p> <p>1:38-42; 1:56-59-2:6; 2:54-62; 3:33-54, 3:60-63; 4:45-58; 5:58-6:17; 6:25-59; 7:3-15; 7:23-29; Figs. 1, 4-7; Abstract.</p>	<p>forming a plurality of row intersecting pixel activation lines and column intersecting pixel activation lines</p> <p><u>Intrinsic Support</u></p> <p>6:1-18; 6:26-36; 5:58-68; 6:38-50; 7:3-10; and figures referenced therein</p>	<p>forming a plurality of row intersecting pixel activation lines and a plurality of column intersecting pixel activation lines</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 1, 4, 5, &amp; 6; 3:25-4:3; 5:44-7:10</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another	A	<p>electrically connecting with conductive material all or nearly all row lines to at least one other row line and electrically connecting with conductive material all or nearly all of the column lines to at least one other column line</p> <p><u>Intrinsic Support</u></p> <p>1:34-35; 5:65-68; 6:6-17; 6:26-32; 6:38-60; 8:1-37; 8:49-62, Fig. 4-7.</p>	<p>electrically connecting with conductors nearly all, but not all, of said row lines to one another and nearly all, but not all, of said column lines to one another</p> <p><u>Intrinsic Support</u></p> <p>5:65-68; 6:6-9; 6:42-43; 8:5-7; and figures referenced therein see also June 13, 2006 Memorandum Opinion 4-6</p>	<p>joining almost all of the row lines together and joining almost all of the column lines together</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 1, 4, 5, 6 &amp; 7; 3:25-4:3; 5:44-7:10; 8:1-48; U.S. Pat. No. 4,820,222; Figs. 1, 6, 7, &amp; 8; 7: 39-8:34 App 07/218312, 3/31/89 OA, Pages 2-3; App 07/218312, 6/25/90 Proposed Response, Pages 2-3 App 06/948224, 3/16/88 Office Action, Pages 3-4; App 06/948224, 9/16/88 Response, Pages 7-9</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
interconnecting	L C	electrically connecting with conductive material  <u>Intrinsic Support</u>  1:34-35; 5:65-68; 6:6-17; 6:26-32; 6:38-60; 8:1-37; 8:49-62, Fig. 4-7; App 07/218,312, 3/31/1989, Office Action, pages 2-4; App 07/218,312, 7/12/1990, Response, pages 2-3.	electrically connecting with conductors  <u>Intrinsic Support</u>  5:65-68; 6:6-9; 6:42-43; 8:5-7; and figures referenced therein see also June 13, 2006 Memorandum Opinion 4-6	Joining together  <u>Intrinsic Support</u>  E.g., Figs. 1, 4, 5, 6 & 7; 3:25-4:3; 5:44-7:10; 8:1-48 U.S. Pat. No. 4,820,222: Figs. 1, 6, 7, & 8; 7: 39-8:34 App 07/218312, 3/31/89 OA, Pages 2-3 App 07/218312, 6/25/90 Proposed Response, Pages 2-3 App 06/948224, 3/16/88 Office Action, Pages 3-4; App 06/948224, 9/16/88 Response, Pages 7-9
substantially all	C A	all or nearly all  <u>Intrinsic Support</u>  1:34-35; 5:65-68; 6:6-17; 6:26-32; 6:38-60; 8:1-37; 8:49-62; Fig. 4-7.	nearly all, but not all  <u>Intrinsic Support</u>  1:15-35; 1:56-2:10; 2:45-51; 4:9-31; and figures referenced therein	Almost all  <u>Intrinsic Support</u>  E.g., Figs. 1, 4, 5, 6 & 7; 3:25-4:3; 5:44-7:10; 8:1-48 U.S. Pat. No. 4,820,222: Figs. 1, 6, 7, & 8; 7:39-8:34

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
row lines	C	electrically conductive material patterned in rows that control pixels  <u>Intrinsic Support</u>  1:38-42; 1:56-59-2:6; 2:54-62; 3:33-54, 3:60-63; 4:45-58; 5:58-6:17; 6:25-59; 7:3-15; 7:23-29; Figs. 1, 4-7; Abstract.	Indefinite  or  lines connecting all pixels in a row  <u>Intrinsic Support</u>  1:38-42; 3:37-46; and figures referenced therein	Indefinite; or Lines connecting all pixels in a row  <u>Intrinsic Support</u>  E.g., Figs. 1, 4, 5, 6 & 7; 3:25-4:3; 5:44-7:10; 8:1-48 U.S. Pat. No. 4,820,222; Figs. 1, 6, 7, & 8; 7: 39-8:34
column lines	C	electrically conductive material patterned in columns that control pixels  <u>Intrinsic Support</u>  1:38-42; 1:56-59-2:6; 2:54-62; 3:33-54, 3:60-63; 4:45-58; 5:58-6:17; 6:25-59; 7:3-15; 7:23-29; Figs. 1, 4-7; Abstract.	indefinite  or  lines connecting all pixels in a column  <u>Intrinsic Support</u>  1:38-42; 3:37-46; and figures referenced therein	Indefinite; or Lines connecting all pixels in a column  <u>Intrinsic Support</u>  E.g., Figs. 1, 4, 5, 6 & 7; 3:25-4:3; 5:44-7:10; 8:1-48 U.S. Pat. No. 4,820,222; Figs. 1, 6, 7, & 8; 7:39-8:34

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
row and column lines	C	<p>electrically conductive material patterned in rows and columns that control pixels</p> <p><u>Intrinsic Support</u></p> <p>1:38-42; 1:56-59-2:6; 2:54-62; 3:33-54, 3:60-63; 4:45-58; 5:58-6:17; 6:25-59; 7:3-15; 7:23-29; Figs. 1, 4-7; Abstract.</p>	<p>Indefinite or the row lines and the column lines</p> <p><u>Intrinsic Support</u></p> <p>1:38-42; 3:37-46; and figures referenced therein</p>	<p>Indefinite; or The row lines and the column lines</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 1, 4, 5, 6 &amp; 7; 3:25-4:3; 5:44-7:10; 8:1-48 U.S. Pat. No. 4,820,222: Figs. 1, 6, 7, &amp; 8; 7:39-8:34</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
outer electrostatic discharge guard ring	L C A	<p>a closed or open ring, or open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharge</p> <p><u>Intrinsic Support</u></p> <p>1:8-14; 2:37-68; 3:20-21; 4:22-31; 4:46-60; 7:11-22; 7:30-34; 8:1-17; 8:24-37; 8:40-44; 8:49-62; Abstract; Figs. 5-7; App 07/218,312, 3/31/1989, Office Action, pages 2-4; App 07/218,312, 7/12/1990, Proposed Response, page 2-3.</p>	<p>a closed or open ring, or open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharges</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:61-62; 8:27-29; and figures referenced therein see also June 13, 2006 Memorandum Opinion 7-10</p>	<p>A surrounding structure outside the active matrix display to provide protection from electrostatic discharges</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 4, 5, 6 &amp; 7; 3:25-4:3; 5:44-7:10; 8:1-48</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
resistance	L C A	<p>a circuit component designed to provide opposition to electric current flowing through itself and to minimize current surge in the TFT array from electrostatic discharge</p> <p><u>Intrinsic Support</u></p> <p>1:8-14; 2:45-68; 4:46-60; 5:32-43; 7:14-18; 7:35-46; 7:61-68; 8:18-39; 8:49-62; Abstract; App 07/218,312, 3/31/1989, Office Action, pages 2-4; App 07/218,312, 7/12/1990, Response, pages 2-3.</p>	<p>a circuit component that has a specified resistance to the flow of electric current and is used to minimize the current surge from an electrostatic discharge</p> <p><u>Intrinsic Support</u></p> <p>8:23-34; and figures referenced therein see also June 13, 2006 Memorandum Opinion 10-13</p>	<p>A circuit component that has a specified ratio between voltage and the flow of electric current, and used to minimize the current surge from electrostatic discharge.</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 4, 5, 6 &amp; 7; 3:25-4:3; 5:44-7:10; 8:1-48</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays	A	<p>to minimize current surge in the TFT array from electrostatic discharge during manufacture of the display</p> <p><u>Intrinsic Support</u></p> <p>1:8-14; 2:45-68; 4:46-60; 5:32-43; 7:14-18:7:35-46; 7:61-68; 8:23-39; 8:49-62; Abstract; Fig. 5, 7.</p>	Indefinite	<p>To guard against electrostatic discharges between the row activation lines and column activation lines during the manufacturing of the displays</p> <p><u>Intrinsic Support'</u></p> <p>E.g., 4:9-6:59; 9:1-48</p>
protection from electrostatic discharges	C	<p>to minimize current surge in the TFT array from electrostatic discharge during manufacture of the display</p> <p><u>Intrinsic Support</u></p> <p>1:8-14; 2:45-68; 4:46-60; 5:32-43; 7:14-18:7:35-46; 7:61-68; 8:23-39; 8:49-62; Abstract; Fig. 5, 7.</p>	Indefinite	<p>Plain meaning; or Guarding against electrostatic discharges</p> <p><u>Intrinsic Support</u></p> <p>E.g., 4:9-6:59; 8:1-48</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
row and column activation lines	C	electrically conductive material patterned in rows and columns that control pixels  <u>Intrinsic Support</u>  1:38-42; 1:56-59-2:6; 2:54-62; 3:33-54, 3:60-63; 4:45-58; 5:58-6:17; 6:25-59; 7:3-15; 7:23-29; Figs. 1, 4-7; Abstract.	indefinite  or  control lines activating all pixels in rows and control lines activating all pixels in columns  <u>Intrinsic Support</u>  1:38-42; 2:4-7; 3:37-46; and figures referenced therein	Indefinite;  or  Control lines activating all pixels in rows and control lines activating all pixels in columns.  <u>Intrinsic Support</u>  E.g., 4:9-6:59; 8 : 1-48
removing said outer guard ring and row and column interconnections	L C	physically disconnecting said guard ring and row and column interconnections  <u>Intrinsic Support</u>  2:45-68; 8:11-17; 8:26-30; 8:40-62; Abstract; App 07/218,312, 3/31/1989, Office Action, pages 2-4; App 07/218,312, 7/12/1990, Response, pages 2-3.	physically disconnecting said guard ring and row and column interconnections  <u>Intrinsic Support</u>  Abstract; 2:64-65; 8:27-30; and figures referenced therein	Indefinite; physically disconnecting said guard ring and lines connecting the row and column , intersecting pixel activation lines from the substrate  <u>Intrinsic Support</u>  E.g., Fig. 7; 2:45-68; 8:1-48 App 07/218312, 3/31/89 OA, Pages 2-3 App 07/218312, 6/25/90 Proposed Response, Pages 2-3 U.S. Pat. No. 4,820,222; Figs. 6 & 8; 6: 42-7:38

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT B**  
**LG DISPLAY USP 5,019,002**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
removing	A	<p>physically disconnecting said guard ring and row and column interconnections</p> <p><u>Intrinsic Support</u></p> <p>2:45-68; 8:11-17; 8:26-30; 8:40-62; Abstract; App 07/218,312, 3/31/1989, Office Action, pages 2-4; App 07/218,312, 7/12/1990, Response, pages 2-3.</p>	<p>physically disconnecting</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:64-65; 8:27-30; and figures referenced therein</p>	<p>Taking away</p> <p>Alternate 1: separating or breaking off</p> <p>Alternate 2: physically disconnecting</p> <p><u>Intrinsic Support</u></p> <p>E.g., Fig. 7; 2:45-68; 8:1-48 App 07/218312, 2/31/89 OA, Pages 2-3 App 07/218312, 7/22/90 Proposed Response, Pages 2-3 U.S. Pat. No. 4,820,222: Figs. 6 &amp; 8; 6: 42-7:38</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT B**  
**LG DISPLAY USP 5,019,002**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
inner electrostatic discharge guard ring	L C	<p>a closed or open ring, or open L or C-shaped line, inside the source and/or gate pads to provide protection from electrostatic discharge</p> <p><u>Intrinsic Support</u></p> <p>1:8-14; 2:45-68; 4:46-60; 5:32-43; 6:60-72; 7:14-68; 8:49-62, Abstract.</p>	<p>a closed or open ring, or open L or C-shaped conductive line, inside the active matrix display to provide protection from electrostatic discharges</p> <p><u>Intrinsic Support</u></p> <p>7:14-21; 7:22-68; and figures referenced therein see also June 13, 2006 Memorandum Opinion 7-10; LGD's Mar. 8, 2006 Plaintiffs Memorandum in Support of Its Proposed Claim Constructions 15-17</p>	<p>Ring structure inside the active matrix display to provide protection from electrostatic discharges</p> <p><u>Intrinsic Support</u></p> <p>E.g., Fig. 5; 2:45-68; 6:60-7:68</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT B**  
**LG DISPLAY USP 5,019,002**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
shunt switching elements	C A	shunt transistors, including floating gate, no gate, an oxide below to form a spark gap, or other active switching elements such as diodes  <u>Intrinsic Support</u>  7:22-50; 7:61-68; 8:49-62; Abstract.	an active switching element like a shunt transistor or diode  <u>Intrinsic Support</u>  8:57-59; 8:18-27; 8:34-39; and figures referenced therein see also LGD's Mar. 8, 2006 Plaintiff's Memorandum in Support of Its Proposed Claim Constructions 19-20.	A switching circuit for shunting electrostatic discharges  <u>Intrinsic Support</u>  E.g., Fig. 5; 2:45-68; 6:60-7:68

# **EXHIBIT C**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT C**  
**LG DISPLAY USP 5,825,449**

<b>Claim Terms</b>	<b>Des.</b>	<b>Agreed Constructions</b>
substrate	C	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.
indium tin oxide layer	C	a thickness of indium tin oxide (ITO)
contact hole is provided through ... layer(s)	C A	the contact hole is formed in the layer(s)

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
wiring structure	C	a structure electrically connecting at least two points  <u>Intrinsic Support</u>  4:24-27; Figs. 1-3.	a structure providing an electrically conductive path that connects at least two terminals  <u>Intrinsic Support</u> 1:52-54; 2:16-18; 4:1-5; 4:24-26; Figs. 4, 6; 5/5/05 Order re Claim Construction, Case No. 02 6775, at 13; Second Revised Joint Claim Construction Statement, Case No. 02 6775, at 179	A structure made by wires  <u>Intrinsic Support</u>  E.g., Figs. 2-5; 2:31-3:14

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT C**  
**LG DISPLAY USP 5,825,449**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
conductive layer	L C	thickness of electrically conductive material  <u>Intrinsic Support</u>  1:34-38; 2:31-3:15; 3:44-50; 4:50-53; 4:65-5:22; Fig 1-3.	a thickness of electrically conductive material that may include one or more patterned features, all of a single material  <u>Intrinsic Support</u>  1:34-37; 1:56-60; 1:61-64; 2:37-46; 3:44-47; 4:50-53; 4:61-5:22; 7:36-39 (claim 10); Figs. la, le, 2a, 2e, 3; '449 File history, 8/1/97 Office Action, para. 2.	Plain meaning
layer	C	a thickness of material  <u>Intrinsic Support</u>  1:34-38; 2:31-3:15; 3:44-50; 4:50-53; 4:65-5:22; Fig 1-3.	plain meaning	Plain meaning
formed on a first portion of said substrate	C	above and in contact with a first part of the substrate  <u>Intrinsic Support</u>  1:31-48; 1:56-64; 2:37-46; 3:44-62; 4:19-23; 4:39-41; 4:65-5:8; Figs 2-3; App. No. 08/781,188, 8/1/97, Office Action, page 2.	above and in contact with a first part of the substrate  <u>Intrinsic Support</u>  1:56-60; Figs. la, le, 2a, 2e, 3	Produced above, supported by, and in contact with a first portion of the substrate  <u>Intrinsic Support</u>  E.g., Figs. 3, 4, & 5; 4:46-4:64; 4:65-5:5; 5:23-38; 5:39-54

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT C**  
**LG DISPLAY USP 5,825,449**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
formed on	C A	above and in contact with  <u>Intrinsic Support</u>  1:31-48, 56-64; 2:37-46; 3:44-62; 4:19-23; 4:39-41; 4:65-5:8; Figs 2-3; App. No. 08/781,188, 8/1/97, Office Action, page 2.	above and in contact with  <u>Intrinsic Support</u>  1:35-38, 1:42-44, 1:44-48, 2:37-40, 2:42-44, 3:44-47, 3:56-60; Figs. 1a-1f, 2a-2e, 3	Produced above, supported by, and in contact with  <u>Intrinsic Support</u>  E.g., Figs. 3, 4, & 5; 4:46- 4:64; 4:65-5:5; 5:23-38; 5:39-54
formed on a second portion of said substrate	C	above and in contact with a second part of the substrate  <u>Intrinsic Support</u>  1:31-48, 56-64; 2:37-46; 3:44-62; 4:19-23; 4:39-41; 4:65-5:8; Figs 2-3; App. No. 08/781,188, 8/1/97, Office Action, page 2.	above and in contact with a second part of the substrate  <u>Intrinsic Support</u>  1:35-38, 3:44-47; Figs. 2b, 3	Produced above, supported by, and in contact with a second portion of the substrate  <u>Intrinsic Support</u>  E.g., Figs. 3, 4, & 5; 4:46- 4:64; 4:65-5:5; 5:23-38; 5:39-54

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT C**  
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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
formed on a first portion of said first insulative layer	C	<p>above and in contact with a first part of the first insulative layer</p> <p><u>Intrinsic Support</u></p> <p>1:31-48, 56-64; 2:37-46; 3:44-62; 4:19-23; 4:39-41; 4:65-5:8; Figs 2-3; App. No. 08/781,188, 8/1/97, Office Action, page 2.</p>	<p>above and in contact with a first part of the first insulative layer</p> <p><u>Intrinsic Support</u></p> <p>1:42-44; Figs. 2b, 3, 5</p>	<p>Produced above, supported by, and in contact with a first portion of the first insulative layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 4:46-4:64; 5:6-5:15; 5:23-38; 5:39-54</p>
insulative layer	C	<p>a thickness of non-conductive material (such as SiNx) that has high electrical resistance</p> <p><u>Intrinsic Support</u></p> <p>1:40-42; 2:5-9, 2:40-41, 45-51, 61-62; 3:1-8, 50-54; 4:6-12, 27-34, 47-50; 5:1-2, 8-15; Figs. 1-3.</p>	Plain meaning	Plain meaning

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT C**  
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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer	C	above and in contact with the second conductive layer and above and in contact with a second part of the first insulative layer above the first conductive layer  <u>Intrinsic Support</u>  1:31-48, 56-64; 2:37-46; 3:44-62; 4:19-23; 4:39-41; 4:65-5:8; Figs 2-3; App. No. 08/781,188, 8/1/97, Office Action, page 2.	above and in contact with the second conductive layer and above and in contact with a second part of the first insulative layer above the first conductive layer  <u>Intrinsic Support</u>  Figs. 1f, 2d, 3 (e.g., element 9)	Produced above, supported by, and in contact with the second conductive layer and a second portion of the insulative layer covering the top surface of the first conductive layer  <u>Intrinsic Support</u>  E.g., Figs. 3, 4, & 5; 4:46-4:64; 5:6-5:15; 5:23-38; 5:39-54
overlying	C	above	this term should be construed as part of the larger term ("formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer")  <u>Intrinsic Support</u>  1:40-44; 2:37-55; 3:63-4:15; 5:16-22; Figs 1-3.	Covering the top surface of  <u>Intrinsic Support</u>  E.g., Figs. 3, 4, & 5; 4:46-4:64; 5:6-5:15; 5:23-38; 5:39-54

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT C**  
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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
contact hole	C	<p>an opening in one or more insulative layers to expose a portion of a conductive layer for purposes of forming an electrical connection.</p> <p><u>Intrinsic Support</u></p> <p>1:51-2:10; 2:31-3:14; 3:50-4:41; 4:47-5:47; Figs. 1-3.</p>	<p>an opening formed in one or more insulative layers to expose a portion of a conductive layer for purposes of forming an electrical connection</p> <p><u>Intrinsic Support</u></p> <p>2:46-55, 3:2-14, 4: 8-15, 4: 53-64, 5:8-13, 5:19-22, 5:33-36; Figs. 2d-2e, 3 and 5</p>	Plain meaning
provided through	C	<p>the contact hole is formed in the layer</p> <p><u>Intrinsic Support</u></p> <p>1:51-2:10; 2:31-3:14; 3:50-4:41; 4:47-5:47; Figs. 1-3.</p>	plain meaning	See above
expose part of said ... layer	C	<p>removing portions of one or more layers to uncover at least part of another layer</p> <p><u>Intrinsic Support</u></p> <p>1:52-60; 2:5-10, 17-28, 45-55; 3:1-14, 3:66-4:15; 4:35-39, 46-50; 5:8-22; Figs. 1-3; Abstract.</p>	plain meaning	Plain meaning

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT C**  
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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
extends through	C	is disposed in  <u>Intrinsic Support</u>  1:50-60; 2:36-3:15; 4:16-34; 4:47-64; 5:5-23; Figs 1-3.	plain meaning	Plain meaning
one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor	C A	one, but not both, of the first and second conductive layers is directly connected to one terminal of a thin film transistor  <u>Intrinsic Support</u>  1:24-30; 2:31-3:15; 3:63-4:5; 4:46-5:23; Fig 3; App. No. 08/781,188, 12/1/1997, Amendment, at p. 5-7.	the first conductive layer is connected to the gate, source or drain of a thin film transistor, and/or the second conductive layer is connected to the gate, source or drain of the thin film transistor  <u>Intrinsic Support</u>  2:16-28, 4:1-5; 4:65-5:13; 5:16-22; 5:23-39; 5:40-51, Figs. 3, 4, 5; '449 File history, 8/1/97 Office Action, para. 6; '449 File history, 12/1/1997 Amendment & Response, pages 1-7; Claims 2, 6; Specification pages 16-17.	At least one of the first and second conductive layers is electrically connected to at least one of the source, drain, and gate electrodes of a thin film transistor.  <u>Intrinsic Support</u>  E.g., Figs. 3, 4, & 5; 4:46-5:53; 5:23-53 App 08/781,188, 12/01/97 Response, pg. 1-7

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT C**  
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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
one of said first and second conductive layers	C	<p>one, but not both, of the first and second conductive layers</p> <p><u>Intrinsic Support</u></p> <p>4:46-5:23; Fig 3; App. No. 08/781,188, 12/1/1997, Amendment, at p. 5-7.</p>	<p>this term should be construed as part of the larger term "one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor"</p>	<p>At least one of the first and second conductive layers</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 4:46-5:53; 5:23-53 App 08/781,188, 12/01/97 Response, pg. 1-7</p>
one	L	<p>a single layer</p> <p><u>Intrinsic Support</u></p> <p>4:46-5:23; Fig 3; App. No. 08/781,188, 12/1/1997, Amendment, at p. 5-7.</p>	<p>this term should be construed as part of the larger term "one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor"</p>	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 4:46-5:53; 5:23-53 App 08/781,188, 12/01/97 Response, pg. 1-7</p>
connected to	C A	<p>directly connected to</p> <p><u>Intrinsic Support</u></p> <p>1:24-30; 2:31-3:15; 3:63-4:5; 4:46-5:23; Fig 3; App. No. 08/781,188, 12/1/1997, Amendment, at p. 5-7.</p>	plain meaning	<p>Electrically connected to</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4 &amp; 5; 4:46-5:53; 5:23-53</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT C**  
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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
one of a plurality of terminals of a thin film transistor	L	<p>one of the terminals (i.e., source, drain, or gate) of a thin film transistor</p> <p><u>Intrinsic Support</u></p> <p>4:46-5:23; Fig 3; App. No. 08/781,188, 12/1/1997, Amendment, at p. 5-7.</p>	<p>this term should be construed as part of the larger term "one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor"</p>	<p>At least one of the source, gate, and drain electrodes of a thin film transistor</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 4:46-5:53; 5:23-53 App 08/781,188, 12/01/97 Response, pg. 1-7</p>
a plurality of terminals of a thin film transistor	C	<p>the terminals (i.e., source, drain, or gate) of a thin film transistor</p> <p><u>Intrinsic Support</u></p> <p>4:46-5:23; Fig 3; App. No. 08/781,188, 12/1/1997, Amendment, at p. 5-7.</p>	<p>this term should be construed as part of the larger term "one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor"</p> <p>to the extent that the embedded term "terminals of a thin film transistor" needs to be construed, CMO proposes the following construction:</p> <p>the gate, source, and drain of a thin film transistor</p> <p>'449 File history, 12/1/1997 Amendment &amp; Response, page 5</p>	<p>Source, drain, and gate electrodes of a thin film transistor</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 4:46-5:53; 5:23-53 App 08/781,188, 12/01/97 Response, pg. 1-7</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT C**  
**LG DISPLAY USP 5,825,449**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
thin film transistor	C	<p>A three terminal device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than in a single crystal silicon wafer</p> <p><u>Intrinsic Support</u></p> <p>1:22-33; Figs 1-3; App. No. 08/781,188, 12/1/1997, Amendment, at p. 5-7.</p>	<p>A three terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than in a single crystal silicon wafer.</p> <p><u>Intrinsic Support</u></p> <p>1:13-30; Figs. 1f, 2e, 3, 4; 5/5/05 Order re Claim Construction, Case No. 02 6775, at 13; Second Revised Joint Claim Construction Statement, Case No. 02- 6775, at 157-159; '449 Prosecution History, 12/1/1997 Amendment &amp; Response, page 5</p>	<p>A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT C**  
**LG DISPLAY USP 5,825,449**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
liquid crystal display device	C	<p>a type of display that generates an image by directing light through an array of liquid crystal pixels, where the amount of light effused by each pixel is controlled via an electric field varying the orientation of the liquid crystal molecules contained within the pixel</p> <p><u>Intrinsic Support</u></p> <p>1:8-25; 1:31-34; Fig. 1-3.</p>	<p>a type of display that generates an image by directing light through an array of liquid crystal pixels, where the amount of light effused by each pixel is controlled via an electric field varying the orientation of the liquid crystal molecules contained within the pixel</p> <p><u>Intrinsic Support</u></p> <p>1:13-30; Fig. 6</p>	Plain meaning
gate electrode	C A	<p>a patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>1:22-38; 56-60; 2:37-44; 2:56-61; 3:44-49; 4:47-53; 4:65-5:1; 5:29-38; Figs. 1-3.</p>	<p>a patterned, electrically conductive material that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>Figs. 1a, 1e, 2a, 2e, 3 (e.g., element 2); 3:44-49; see also 1:34-37; 2:37-44; 2:56 - 3:1; 5:29-38.</p>	<p>A patterned, electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode</p> <p><u>Intrinsic Support</u></p> <p>E.g., Fig. 3; 2:37-3:14 (Summary of the Invention)</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT C**  
**LG DISPLAY USP 5,825,449**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
gate pad	C A	<p>a portion of patterned electrically conductive material that is provided near the periphery of the thin film transistor array to receive a gate signal</p> <p><u>Intrinsic Support</u></p> <p>1:22-38; 1:52-60; 2:8-10; 2:19-26; 3:44-49; 4:6-15; 4:21-27; 4:35-41; 4:47-53; 4:65-5:1; 5:19-23; Figs. 1, 3.</p>	<p>a portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive a gate signal from a gate driving circuit</p> <p><u>Intrinsic Support</u></p> <p>Figs. 1a-1e, 2a-2e (e.g., element 2C), 3 (e.g., element 2B), 6; 1:27-30; 1:34-38; 1:52-55; 2:39-40; 2:59-61; 4:8-15; 4:47-53; 4:65-5:1.</p> <p>5/5/05 Order re Claim Construction, Case No. 02 6775, at 17; Second Revised Joint Claim Construction Statement, Case No. 02 6775, at 162-165.</p>	<p>a patterned, electrically, conductive material that is provided near the periphery of the thin film transistor array to receive a gate signal from a gate driving circuit</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 4:65-5:5; 5:23-38; 5:39-54</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT C**  
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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
source pad	L C A	<p>a portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive a data signal</p> <p><u>Intrinsic Support</u></p> <p>1:8-12; 1:22-38; 1:52-64; 2:8-10; 2:17-22; 3:66-4:5; 4:6-14; 4:24-27; 4:35-61; 4:65-5:1; 5:19-23; 5:48-51; Figs. 1-3.</p>	<p>a portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive a data signal from a data driving circuit</p> <p><u>Intrinsic Support</u></p> <p>Figs. 1a–1e, 2a–2e, 3 (e.g., element 2A), 6; 1:27-30; 1:34-38; 1:52-55; 1:67 – 2:4; 4:8-15.</p> <p>5/5/05 Order re Claim Construction, Case No. 02 6775, at 17; Second Revised Joint Claim Construction Statement, Case No. 02 6775, at 165-168..</p>	<p>a patterned, electrically, conductive material that is provided near the periphery of the thin film transistor array to receive a data signal from a data driving circuit</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 4:65-5:5; 5:23-38; 5:39-54</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT C**  
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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
a gate insulating film on said surface of said substrate	C	<p>a thickness of non-conductive material (such as SiNx) that has high electrical resistance and insulates the transistor gate from the semiconductor above and in contact with at least part of the surface of the substrate</p> <p><u>Intrinsic Support</u></p> <p>1:52-55; 2:11-13; 2:19-26; 2:34-36; 2:40-44; 3:50-53; 4:1-15; 4:35-39; 4:47-50; 4:65-5:4; 5:12-15; 5:19-23; 5:40-46; Figs. 1-3.</p>	plain meaning	<p>A gate insulating film above, supported by, and in contact with the surface of the substrate</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 4:65-5:5; 5:23-38; 5:39-54</p>
gate insulating film	C	<p>a thickness of non-conductive material (such as SiNx) that has high electrical resistance and insulates the transistor gate from the semiconductor</p> <p><u>Intrinsic Support</u></p> <p>1:52-55; 2:11-13; 2:19-26; 2:34-36; 2:40-44; 3:50-53; 4:1-15; 4:35-39; 4:47-50; 4:65-5:4; 5:12-15; 5:19-23; 5:40-46; Figs. 1-3.</p>	plain meaning	<p>Plain meaning: or Insulating film formed over the gate region</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 4:65-5:5; 5:23-38; 5:39-54</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
insulating film	C	<p>a thickness of non-conductive material (such as SiNx) that has high electrical resistance</p> <p><u>Intrinsic Support</u></p> <p>1:52-55; 2:11-13; 2:19-26; 2:34-36; 2:40-44; 3:50-53; 4:1-15; 4:35-39; 4:47-50; 4:65-5:4; 5:12-15; 5:19-23; 5:40-46; Figs. 1-3.</p>		Plain meaning
a semiconductor layer on said portion of said gate insulating film	C	<p>a thickness of semiconductor material above and in contact with a part of the gate insulating film</p> <p><u>Intrinsic Support</u></p> <p>1:40-51; 1:61-2:4; 2:37-3:15; 3:50-4:5; 4:65-5:5; Figs 1-3.</p>	<p>a thickness of semiconductor material above and in contact with a part of the gate insulating film</p> <p><u>Intrinsic Support</u></p> <p>Figs. 1b-1f, 2b-2e, 3; 1:53-54, 2:42-44; 2:61-64; 3:50-62; 5:1-5</p>	<p>A semiconductor above, supported by, and in contact with the portion of the gate insulating film</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 4:65-5:5; 5:23-38; 5:39-54</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
semiconductor layer	C	<p>a thickness of semiconductor material, such as amorphous silicon</p> <p><u>Intrinsic Support</u></p> <p>1:40-51; 1:61-2:4; 2:37-3:15; 3:50-4:5; 4:65-5:5; Figs 1-3.</p>	<p>a thickness of a semiconductor material, such as amorphous silicon</p> <p><u>Intrinsic Support</u></p> <p>1:53-54, 2:42-44; 5:1-5; Figs. 1b – If, 2b – 2e, 3</p>	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 4:65-5:5; 5:23-38; 5:39-54</p>
impurity-doped semiconductor layer	C	<p>a thickness of semiconductor material, such as amorphous silicon, to which impurities (such as phosphorous atoms) have been added to enhance electrical conductivity</p> <p><u>Intrinsic Support</u></p> <p>1:40-51; 1:61-2:4; 2:37-3:15; 3:50-4:5; 4:65-5:5; Figs 1-3.</p>	<p>a thickness of semiconductor material, such as amorphous silicon, to which impurities (such as phosphorous atoms) have been added to enhance electrical conductivity</p> <p><u>Intrinsic Support</u></p> <p>1:43-48, 3:52-63; 5:1-5; Figs. 2b – 2e, 3 (e.g., element 5)</p>	<p>Plain meaning;</p> <p>or</p> <p>Semiconductor layer doped with impurities</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 4:65-5:5; 5:23-38; 5:39-54</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
a source electrode and a drain electrode on said semiconductor layer	A	<p>a source electrode and a drain electrode above and in contact with the semiconductor layer</p> <p><u>Intrinsic Support</u></p> <p>1:40-51; 1:61-2:4; 2:37-3:15; 3:50-4:5; 4:65-5:15; Figs 1-3.</p>	<p>a source electrode and a drain electrode above and in contact with the semiconductor layer</p> <p><u>Intrinsic Support</u></p> <p>Figs. 1e-1f, 2c-2e, 3 (e.g., source electrode 7 and drain electrode 8)</p> <p>1:44-50; 1:61-67; 3:56-60; 3:63-66; 4:27-34; 5:6-8</p>	<p>The source electrode and the drain electrode above, supported by, and in contact with the semiconductor layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 5:6-5:15; 5:23-38; 5:39-54</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
source electrode	C A	a patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode	Construe term:  "a source electrode and a drain electrode"  as:  Patterned, electrically conductive material formed over the source region and drain region, respectively, of a transistor. Current flows through the channel between the source electrode and the drain electrode of the transistor under control of the gate electrode of the transistor.	A patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
drain electrode	C A	<p>a patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source and drain electrode under the control of the gate electrode</p> <p><u>Intrinsic Support</u></p> <p>1:8-12; 1:22-30; 1:61-2:4; 2:11-27; 2:37-3:15; 3:63-4:5; 4:47-64; 5:6-22; Figs. 1e-1f; 2c-e, 3.</p>	<p>this term should be construed as part of the larger term "a source electrode and a drain electrode" (see above)</p>	<p>A patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 5:6-5:15; 5:23-38; 5:39-54</p>
passivation layer	C	<p>a thickness of insulative material that provides protection such as electrical stability and chemical isolation</p> <p><u>Intrinsic Support</u></p> <p>2:5-10; 2:19-26; 2:34-36; 2:40-46; 3:50-53; 4:1-15; 4:35-39; 4:47-50; 4:65-5:4; 5:12-15; 5:19-23; 5:40-46; Figs. 1-3.</p>	<p>a thickness of insulative material that provides protection such as electrical stability and chemical isolation</p> <p><u>Intrinsic Support</u></p> <p>Figs. 1f, 2d-2e, 3 (e.g., element 9); 2:5-8; 4:6-8; 5:6-15</p>	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 2:37-3:14 (Summary of the Invention); 4:46-4:64; 5:6-5:15; 5:23-38; 5:39-54</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT C**  
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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
exposing said gate pad portion	A	<p>removing portions of one or more layers to uncover at least part of a gate pad [portion]</p> <p><u>Intrinsic Support</u></p> <p>1:52-60; 2:5-10, 17-28, 45-55; 3:1-14, 3:66-4:15; 4:35-65; 5:6-22; Abstract; Figs 1-3.</p>	plain meaning	<p>Causing the gate pad to be exposed to the atmosphere</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 2:37-3:14 (Summary of the Invention); 4:46-5:22</p>
exposing	C	<p>removing portions of one or more layers to uncover at least part of another layer</p> <p><u>Intrinsic Support</u></p> <p>1:52-60; 2:5-10, 17-28, 45-55; 3:1-14, 3:66-4:15; 4:35-65; 5:6-22; Abstract; Figs 1-3.</p>	plain meaning	<p>Laying open or causing to be exposed from above</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 4:46-5:53; 5:23-53</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
pixel electrode	C	<p>a pattern of transparent electrically conductive material that stores charge to drive the liquid crystal material within an individual element of the liquid crystal display device</p> <p><u>Intrinsic Support</u></p> <p>1:24-30; 1:56-2:4; 2:16-28; 2:31-3:15; 3:16-41; 4:54-64; 5:15-22; Figs 1-3.</p>	<p>electrode controlling the brightness of a pixel</p> <p><u>Intrinsic Support</u></p> <p>1:15-19, 1:26-30, 1:56-59, 1:67-2:4</p>	<p>Electrode controlling the brightness of a pixel</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 4:46-4:64; 5:16-23; 5:39-54</p>
transparent conductive layer	C	<p>a thickness of transparent electrically conductive material</p> <p><u>Intrinsic Support</u></p> <p>1:55-60; 4:16-19; 4:39-41; 5:15-22; Figs 1-3.</p>	plain meaning	Plain meaning
a method of manufacturing a liquid crystal display device	C	<p>a process for producing a liquid crystal display device</p> <p><u>Intrinsic Support</u></p> <p>1:8-25; 1:31-34; Fig. 103.</p>	plain meaning	Plain meaning

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
patterning ... to form an active layer	C	<p>the removal of selected portions of the impurity-doped semiconductor layer and the semiconductor layer using etching techniques in order to form an active layer</p> <p><u>Intrinsic Support</u></p> <p>1:34-37; 1:44-50; 1:55-67; 2:16-28; 2:56-3:14; 3:44-4:5; 4:16-24; 4:47-5:22; Figs 1-3.</p>	plain meaning	<p>selectively removing portions of ... using etching techniques in order to form an active region</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 4:46-4:64; 4:65-5:5; 5:23-53</p>
patterning	C	<p>the removal of selected portions of a surface using etching techniques in order to produce a pattern in the remaining material</p> <p><u>Intrinsic Support</u></p> <p>1:34-37; 1:44-50; 1:55-67; 2:16-28; 2:56-3:14; 3:44-4:5; 4:16-24; 4:47-5:22; Figs 1-3.</p>	plain meaning	<p>selectively removing portions of a surface using etching techniques in order to produce a pattern in the remaining material</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 4:46-4:64; 4:65-5:5; 5:23-53</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
active layer	C A	<p>a discrete portion of semiconductor layer that is formed by patterning and located at least in part above the gate electrode. In operation, the discrete portion is penetrated, at least in part, by the electric field introduced by the gate electrode.</p> <p><u>Intrinsic Support</u></p> <p>1:34-51; 1:61-2:4; 2:11-27; 3:44-62; 4:65-5:5; 5:39-47; Figs 1-3.</p>	<p>A discrete portion of the semiconductor layer that is formed by patterning and located along the gate electrode of a thin film transistor. In operation, the discrete portion is penetrated, at least in part, by the electric field introduced by the gate electrode of the thin film transistor.</p> <p><u>Intrinsic Support</u></p> <p>1:42-44; 3:47-49; 3:50-62; 5:1-5</p> <p>5/5/05 Order re Claim Construction, Case No. 02 6775, at 18; Second Revised Joint Claim Construction Statement, Case No. 02 6775, at 176-177.</p>	<p>active region of a thin film transistor</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 4:46-4:64; 4:65-5:5; 5:23-53</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
selectively etching	C	<p>the removing selected portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) in order to produce a desired pattern on the surface</p> <p><u>Intrinsic Support</u></p> <p>1:47-55; 2:8-10; 2:31-36; 2:50-51; 3:59-61; 3:67-4:1; 4:8-19; 4:35-39; 4:47-50; 5:1-15; 5:40-47; Figs 1-3.</p>	plain meaning	<p>selectively removing portions of a surface using etching techniques in order to produce a desired pattern in the remaining material</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, &amp; 5; 4:46-5:53</p>
patterning a pixel electrode electrically connected to said drain electrode	C	<p>the removal of selected portions of a pattern of transparent electrically conductive material to form a pixel electrode that has an electrical conduction path with the drain electrode</p> <p><u>Intrinsic Support</u></p> <p>1:34-37; 1:44-50; 1:55-67; 2:16-28; 2:56-3:14; 3:44-4:5; 4:16-24; 4:47-5:22; Figs 1-3.</p>	plain meaning	<p>selectively removing portions of a pixel electrode using etching techniques in order to electrically connect the pixel electrode to the drain electrode</p> <p><u>Intrinsic Support</u></p> <p>E.g., , Figs. 3, 4, &amp; 5; 4:46-5:53</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
electrically connect/electrically connecting/electrically connected	A	provide an electrical conduction path  <u>Intrinsic Support</u>  1:24-30; 2:31-3:15; 4:56-64; 5:8-22; Figs 1-3.	plain meaning	Plain meaning

# **EXHIBIT D**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT D**  
**LG DISPLAY USP 6,664,569**

<b>Claim Terms</b>	<b>Des.</b>	<b>Agreed Constructions</b>
drain electrode	A	A patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.
source electrode	A	A patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
the gate line having an opening therein	A	<p>the gate line has a space in its pattern to reduce gate-drain capacitance and compensate for gate-drain layer misalignment</p> <p><u>Intrinsic Support</u></p> <p>1:13-16; 1:67-2:11; 2:23-67; 3:2-6; 3:30-48; 4:6-11; 4:20-40; 4:47-5:2; 5:41-6:17; 6:21-41; 7:40-57; 7:60-8:28; 8:36-9:17; Abstract; Figs. 4-9; App. No. 09/867,484, 03/13/2003, Office Action; pages 3-4; App. No. 09/867,484, 5/6/2003, Interview Summary; App. No. 09/867,484, 5/8/2002, Response, page 10-11.</p>		<p>Gate line with a cut out extending from the periphery of the gate line to the interior of the gate line</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 5-8; Abstract; 4:63-65; 6:13-15; 6:31-41; 8:7-10; 8:37-42; 7:6-17; 7:41-43; App 09/867484, 5/12/03, Response, pages 10-11</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
a gate line	L	<p>a pattern of electrically conductive material that conveys gate signals to transistors, a portion of which controls current flow through the channel between the source and drain electrodes</p> <p><u>Intrinsic Support</u></p> <p>1:67-2:11; 2:23-35; 2:63-67; 3:2-6; 3:30-48; 5:41-6:17; 6:21-41; 7:60-8:4; 8:36-42; 8:63-9:17; Abstract; Figs. 4-9; App. No. 09/867,484, 03/13/2003, Office Action; pages 3-4; App. No. 09/867,484, 5/6/2003, Interview Summary; App. No. 09/867,484, 5/8/2002, Response, page 10-11.</p>		<p>An elongated directional conductor that supplies signals to gate electrodes</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 1, 2, 7, 8; 2:23-25; 5:40-53; 8:37-42; 1:65-2:8; 2:63-65</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT D**  
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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
having an opening therein	L	<p>has a space in its pattern to reduce gate-drain capacitance and compensate for gate-drain layer misalignment</p> <p><u>Intrinsic Support</u></p> <p>1:13-16; 2:23-3:67; 4:6-11; 4:20-40; 4:47-5:2; 5:47-57; 5:66- 6:17; 6:28-41; 7:40-57; 8:2-28; 8:41-9:17; Abstract; Figs. 5-9; App. No. 09/867,484, 03/13/2003, Office Action; pages 3-4; App. No. 09/867,484, 5/6/2003, Interview Summary; App. No. 09/867,484, 5/8/2002, Response, page 10-11.</p>		<p>Having a cut out extending from the periphery to a point within</p> <p><u>Intrinsic Support</u></p> <p>See support for limitation "the gate line having an opening therein"</p>
a semiconductor layer on the first insulating layer over at least a portion of the opening	A	<p>a layer of semiconductor material, above and supported by or in contact with the first insulating layer, a portion of which overlaps part of the space in the gate line</p> <p><u>Intrinsic Support</u></p> <p>4:30-40; 6:29-58; 7:6-24; 8:1-13; Fig. 4-9; Abstract.</p>		<p>A semiconductor layer above, supported by, and in contact with the first insulating layer, the semiconductor layer being over at least a portion of the opening in the gate line</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 6A, 8 and 9; 6:47-54</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT D**  
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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
a drain electrode on the semiconductor layer over at least a portion of the opening	A	<p>a drain electrode, above and supported by or in contact with the semiconductor layer, a portion of which overlaps part of the space in the gate line</p> <p><u>Intrinsic Support</u></p> <p>2:6-11; 2:24-3:29; 3:36-40; 3:48-67; 4:9-11; 4:32-40; 4:48-65; 5:54-6:17; 6:64-7:23; 7:41-8:28; 8:37-9:17; Figs. 4, 6b, 6c-9; Abstract .</p>		<p>A drain electrode above, supported by, and in contact with the semiconductor layer, the drain electrode being over at least a portion of the opening in the gate line</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 6A, 8 and 9, 7:48-51; 7:6-20</p>
pixel electrode	A	<p>a pattern of transparent electrically conductive material that stores charge to drive the liquid crystal material within an individual element of the liquid crystal display device</p> <p><u>Intrinsic Support</u></p> <p>1:37-65; 2:13-22; 7:33-39; Fig 1, 2, 9.</p>		<p>Electrode controlling the brightness of a pixel</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 1-5, 6B-6C, 7-9; 1:38-48; 2:13-22; 2:24-39; 4:43-36; 6:61-63; 7:34-40</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT D**  
**LG DISPLAY USP 6,664,569**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
substantially surrounds the drain electrode	A	extending considerably around a portion of the drain electrode  <u>Intrinsic Support</u>  4:20-40; 5:59-65; 6:66-7:7:5; 8:5-10; Abstract; Fig. 5, 6B, 6C, 7, 8.		Surrounds almost all the drain electrode portion  <u>Intrinsic Support</u>  E.g., Figs. 5 6B, 6C; 4:37-40; 5:53-61; 6:66-7:2; 7:18-23; 8:5-7.
substantially	A	considerably  <u>Intrinsic Support</u>  4:20-40; 5:59-65; 6:66-7:7:5; 8:5-10; Abstract; Fig. 5, 6B, 6C, 7, 8.		Almost all  <u>Intrinsic Support</u>  E.g., Figs. 5 6B, 6C, 4:37-40; 5:53-61; 6:66-7:2; 7:18-23; 8:5-7.

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT D**  
**LG DISPLAY USP 6,664,569**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
the gate electrode having an opening therein	A	<p>the gate electrode has a space in its pattern to reduce gate-drain capacitance and compensate for gate-drain layer misalignment</p> <p><u>Intrinsic Support</u></p> <p>1:13-16; 1:67-2:11; 2:23-67; 3:2-6; 3:30-48; 4:6-11; 4:20-40; 4:47-5:2; 5:41-6:17; 6:21-41; 7:40-57; 7:60-8:28; 8:36-9:17; Abstract; Figs. 4-9; App. No. 09/867,484, 03/13/2003, Office Action; pages 3-4; App. No. 09/867,484, 5/6/2003, Interview Summary; App. No. 09/867,484, 5/8/2002, Response, page 10-11.</p>		<p>gate electrode with a cut out extending from the periphery of the gate, line to the interior of the gate line</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 5-8; Abstract; 6:31-41; 8:37-42; Abstract; 4:63-65; 8:7-10; 6:13-15; 7:6-17; 7: 41-43</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT D**  
**LG DISPLAY USP 6,664,569**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
gate electrode	L A	<p>patterned electrically conductive material that includes a portion that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>1:67-2:11; 2:23-35; 2:63-67; 3:2-6; 3:30-48; 5:41-6:17; 6:21-41; 7:60-8:4; 8:36-42; 8:63-9:17; Abstract; Figs. 4-9; App. No. 09/867,484, 03/13/2003, Office Action; pages 3-4; App. No. 09/867,484, 5/6/2003, Interview Summary; App. No. 09/867,484, 5/8/2002, Response, page 10-11.</p>		<p>A patterned, electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-5; 8:64-65; 3:30-40; 4:27-31; 6:27-32. App 09/867484, 5/12/03 Response, pages 10-11</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT D**  
**LG DISPLAY USP 6,664,569**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
the opening includes a first opening portion and a second opening portion	A	<p>the space in the gate electrode pattern includes a first part to primarily compensate for gate-drain layer misalignment and a second part to primarily reduce gate-drain capacitance</p> <p><u>Intrinsic Support</u></p> <p>1:13-16; 2:23-3:67; 4:6-11; 4:20-40; 4:47-5:2; 5:47-57; 5:66- 6:17; 6:28-41; 7:40-57; 8:2-28; 8:41-9:17; Abstract; Figs. 5-9; App. No. 09/867,484, 03/13/2003, Office Action; pages 3-4; App. No. 09/867,484, 5/6/2003, Interview Summary; App. No. 09/867,484, 5/8/2002, Response, page 10-11.</p>		<p>Non-rectangular-shaped opening having two distinct opening portions</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 6A, 6B, 9; Abstract; 4:48-50; 6:32-41; 7:17-18</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT D**  
**LG DISPLAY USP 6,664,569**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
a first opening portion	L	<p>a first part to primarily compensate for gate-drain layer misalignment</p> <p><u>Intrinsic Support</u></p> <p>1:13-16; 2:23-3:67; 4:6-11; 4:20-40; 4:47-5:2; 5:47-57; 5:66- 6:17; 6:28-41; 7:40-57; 8:2-28; 8:41-9:17; Abstract; Figs. 5-9; App. No. 09/867,484, 03/13/2003, Office Action; pages 3-4; App. No. 09/867,484, 5/6/2003, Interview Summary; App. No. 09/867,484, 5/8/2002, Response, page 10-11.</p>		<p>One distinct opening portion</p> <p><u>Intrinsic Support</u></p> <p>See above</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT D**  
**LG DISPLAY USP 6,664,569**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
a second opening portion	L	<p>a second part to primarily reduce gate-drain capacitance</p> <p><u>Intrinsic Support</u></p> <p>1:13-16; 2:23-3:67; 4:6-11; 4:20-40; 4:47-5:2; 5:47-57; 5:66- 6:17; 6:28-41; 7:40-57; 8:2-28; 8:41-9:17; Abstract; Figs. 5-9; App. No. 09/867,484, 03/13/2003, Office Action; pages 3-4; App. No. 09/867,484, 5/6/2003, Interview Summary; App. No. 09/867,484, 5/8/2002, Response, page 10-11.</p>		<p>Another distinct opening portion</p> <p><u>Intrinsic Support</u></p> <p>See above</p>
a first electrode	L	<p>a first portion of the drain electrode to primarily compensate for gate-drain layer misalignment</p> <p><u>Intrinsic Support</u></p> <p>4:48-5:2; 5:4-6:17; 7:6-23; 7:41-59; 8:7-28; 8:34-9:17; Abstract; Figs. 2-925-31, 35-37.</p>		<p>One distinct portion of a single electrode</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 5, 6B, 6C, 7-9; 4:53-60; 7:6-17; 6:6-12</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT D**  
**LG DISPLAY USP 6,664,569**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
a second electrode	L	<p>a second portion of the drain electrode to primarily reduce gate-drain capacitance</p> <p><u>Intrinsic Support</u></p> <p>4:48-5:2; 5:4-6:17; 7:6-23; 7:41-59; 8:7-28; 8:34-9:17; Abstract; Figs. 2-925-31, 35-37.</p>		<p>Another distinct portion of a single electrode</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 5, 6B, 6C, 7-9; 4:53-60; 7:6-17; 6:6-12</p>
a third electrode	L	<p>a third portion of the drain electrode to primarily connect to the pixel electrode</p> <p><u>Intrinsic Support</u></p> <p>2:13-22; 4:41-47; 7:24-39; Abstract; Figs. 2-5, 6B, 6C, 7-9.</p>		<p>The third distinct portion of the single electrode</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 5, 6B, 6C, 7, 8; 5:61-65; 7:29-32</p>
connects	L	<p>joins</p> <p><u>Intrinsic Support</u></p> <p>2:13-22; 4:41-47; 5:61-65; 7:24-39; Figs. 2-5, 6B, 6C, 7-8.</p>		<p>Physically attached</p> <p><u>Intrinsic Support</u></p> <p>E.g., 5, 6B, 6C, 7, 8, 5:57-65</p>

# **EXHIBIT E**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT E**  
**LG DISPLAY USP 6,803,984**

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
a first substrate	C	one of a TFT or color filter substrate  <u>Intrinsic Support</u>  5:11-22; 7:9-13; Figs. 2, 3, and 4.	plain meaning  <u>Intrinsic Support</u>  Abstract, 3:61-65, 5:11-25, 7:17-34, Figs. 2-4	Plain meaning;  or  one of the two opposing substrates of the liquid crystal cell  <u>Intrinsic Support</u>  E.g., 1:38-39, 1:59-61; 7:25-33; Claim 5 and 9
a second substrate	C	the other of the TFT or color filter substrate  <u>Intrinsic Support</u>  5:11-22; 7:9-13; Figs. 2, 3, and 4.	The substrate immediately following the first substrate  <u>Intrinsic Support</u>  Abstract; 3:61-66; 5:11-25; 7:17-34; Figs. 2-4	Plain meaning  or  the other of the two opposing substrates of the liquid crystal cell  <u>Intrinsic Support</u>  See above

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT E**  
**LG DISPLAY USP 6,803,984**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
on a single production process line	L	<p>on a production line where the processing equipment is arranged along a common path for performing the liquid crystal cell processes</p> <p><u>Intrinsic Support</u></p> <p>3:25-42; 5:23-30; 7:9-13, 35-41; Figs. 2, 3, and 4; App 10/124,452, 6/17/04 Notice of Allowability, pages 2-3.</p>	<p>On a line structure for processing the substrates in only one direction without branching</p> <p><u>Intrinsic Support</u></p> <p>Abstract, 3:22-53; 3:61-4:13, 5:23-30, 7:17-43, Figs. 1-4, App. No. 10/128,452, January 6, 2004 Amendment at 4-5</p>	<p>On a production line for processing liquid crystal displays in a single, linear arrangement</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-4; 5:23-27; 7:35-43; Claim 1; App 10/128452, 1/8/04 Amendment</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT E**  
**LG DISPLAY USP 6,803,984**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
passing the first and second substrates through a sealing material coating portion of the single production process line in serial order	C	<p>passing the first and second substrates, one after the other, along a portion of the single production process line where the sealing material is selectively applied</p> <p><u>Intrinsic Support</u></p> <p>3:25-42; 5:11-30, 39-50, 62-6; 6:27-34, 42-6; 7:1-13, 35-41; Figs. 2, 3, and 4; App 10/124,452, 6/17/04 Notice of Allowability, pages 2-3.</p>	<p>Providing the first and second substrates, one after the other without anything in between, in at one end, and out at the other end, of a machine for coating sealing material in the single production process line in which the same order of the first and second substrates is maintained throughout the seal dispensing process</p> <p><u>Intrinsic Support</u></p> <p>Abstract, 2:28-38, 2:54-59, 3:61-4:13; 5:11-30, 5:39-50, 6:27-34, 7:1-8, 7:17-44, Figs. 2-4, App. No. 10/128,452, January 6, 2004 Amendment at 4-5</p>	<p>providing the first and second substrate one after the other, without anything in between; in at one end, and out at the other end in the same order of a machine for coating sealing material on a substrate</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-4; 4:20-25, 5:23-30; 6:19-53; 6:54-7:20; App 10/128452, 1/8/04 Amendment, pages 1-6; App 10/128452, 6/23/04</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT E**  
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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
a sealing material coating portion of the single production process line	A	<p>a portion of the single production process line where the sealing material is selectively applied</p> <p><u>Intrinsic Support</u></p> <p>3:25-42; 5:11-30; 5:39-50; 5:62-66; 6:27-34; 6:42-6; 7:1-13; 7:35-41; Figs. 2, 3, and 4.</p>	<p>a machine for coating sealing material in the single production process line</p> <p><u>Intrinsic Support</u></p> <p>Abstract, 2:28-38, 2:54-59, 3:61-4:13, 5:11-30, 5:39-50, 6:27-34, 7:1-8, 7:17-44, Figs. 2-4, App. No. 10/128,452, January 6, 2004 Amendment at 4-5</p>	<p>A machine for coating sealing material in the single production process line.</p> <p><u>Intrinsic Support</u></p> <p>See above</p>
in serial order	A	<p>one after the other</p> <p><u>Intrinsic Support</u></p> <p>5: 39-50, 55-66; 6:27-46, 62-7; 7:1-13, 21-3.</p>	<p>one after the other one without anything in between</p> <p><u>Intrinsic Support</u></p> <p>Abstract, 3:61-4:13, 5:11-25, 5:41-49, 5:56-61, 6:27-41, 6:62-67, 7:1-8, 7:17-34, Figs. 2-4, App. No. 10/128,452, January 6, 2004 Amendment at 4-5</p>	<p>One after the other without anything in between</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-4; 5:23-27; 7:25-33; 6:19-53 &amp; Fig. 3; 6:54-7:20 &amp; Fig. 4</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT E**  
**LG DISPLAY USP 6,803,984**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
passing the first and second substrates through a liquid crystal dispensing portion of the single production process line in serial order	C	<p>passing the first and second substrates, one after the other, along a portion of the single production process line where liquid crystal is selectively dispensed</p> <p><u>Intrinsic Support</u></p> <p>3:25-42; 5:11-30, 55-66  6:35-46; 6:62-67; 7:9-13;  7:35-41; Figs. 2, 3, and 4;  App 10/124,452, 6/17/04  Notice of Allowability,  pages 2-3.</p>	<p>providing the first and second substrates, one after the other without anything in between, in at one end, and out at the other end, of a machine for dispensing liquid crystal material in the single production process line in which the same order of the first and second substrates is maintained throughout the liquid crystal dispensing process</p> <p><u>Intrinsic Support</u></p> <p>Abstract, 2:28-38,  2:63-3:12, 3:61-4:13, 5:11-  30, 5:56-61, 6:36-41, 6:62-  67, 7:17-34, Figs. 2-4, App.  No.10/128,452, January 6,  2004 Amendment at 4-5</p>	<p>providing the first and second substrate one after the other, without anything in between; in at one end, and out at the other end in the same order of the liquid crystal dispensing machine</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-4; 4:26-30;  6:19-53; 6:54-7:20; App  10/128452, 1/8/04  Amendment, pages 1-6 App  10/128452, 6/23/04 Notice  of Allowability, pages 1-4</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT E**  
**LG DISPLAY USP 6,803,984**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
a liquid crystal dispensing portion of the single production process line	A	<p>a portion of the single production process line where liquid crystal is selectively dispensed</p> <p><u>Intrinsic Support</u></p> <p>3:25-42; 5:11-30; 5:55-66; 6:35-46; 6:62-67; 7:9-13; 7:35-41; Figs. 2, 3, and 4; App 10/124,452, 6/17/04 Notice of Allowability, pages 2-3.</p>	<p>a machine for dispensing liquid crystal in the single production process line</p> <p><u>Intrinsic Support</u></p> <p>Abstract, 2:28-38, 2:63-3:12, 3:61-4:13, 5:11-30, 5:56-61, 6:36-41, 6:62-67, 7:17-34, Figs. 2-4, App. No. 10/128,452, January 6, 2004 Amendment at 4-5</p>	<p>a machine for dispensing liquid crystal on a substrate in the single production process line</p> <p><u>Intrinsic Support</u></p> <p>See above</p>
a pixel region	C	<p>area corresponding to the inside of the sealing material</p> <p><u>Intrinsic Support</u></p> <p>5:40-66; 6:27-46; 6:62-7:13.</p>	<p>an area with pixels</p> <p><u>Intrinsic Support</u></p> <p>2:45-53, 3:6-12, 4:7-11, 5:39-47, 6:27-33; 7:1-5</p>	<p>Area with pixel</p> <p><u>Intrinsic Support</u></p> <p>E.g., 2:48-40; 5:16-18; Claim 7</p>
assembling	C	<p>bringing together</p> <p><u>Intrinsic Support</u></p> <p>1:57-61; 3:13-6; 5:44-7; 6:50-2; Figs. 1, 2, 3, and 4.</p>	Indefinite	Indefinite

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT E**  
**LG DISPLAY USP 6,803,984**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
the liquid crystal is dispensed onto the first substrate at the same time that the second substrate is disposed in the sealing material coating portion	A	<p>a point in time when liquid crystal is being dispensed on the first substrate overlaps with a point in time when the second substrate is located in the portion of the single production process line where the sealing material is selectively applied</p> <p><u>Intrinsic Support</u></p> <p>7:22-34.</p>	<p>when the liquid crystal is dispensed onto the first substrate in the machine for dispensing liquid crystal, the second substrate is located in the machine for coating sealing material</p> <p><u>Intrinsic Support</u></p> <p>7:21-34, Figs. 3-4</p>	<p>when the liquid crystal is dispensed onto the first substrate in the liquid crystal dispensing machine, the second substrate is located in the sealant coating machine</p> <p><u>Intrinsic Support</u></p> <p>E.g., 7:22-33</p>
in serial order in a same cleaning unit	L	<p>one after the other in the same cleaning equipment</p> <p><u>Intrinsic Support</u></p> <p>3:25-42; 3:36-43; 5:26-30; 5:11-30, 55-66 6:35-46; 6:62-67; 7:9-13; 7:35-41; Figs. 2, 3, and 4.</p>	<p>one after the other without anything in between, in a same cleaning machine</p> <p><u>Intrinsic Support</u></p> <p>3:22-42, 5:26-30, 5:33-38, 6:19-27, 6:54-61, Figs. 1-4</p>	<p>cleaning the first substrate and the second substrate one after the other without anything in between in the same cleaning machine</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2-4; 5:23-36; 6:19-21; 6:54-56</p>

# **EXHIBIT F**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F**  
**LG DISPLAY USP 5,905,274**

<b>Claim Terms</b>	<b>Des.</b>	<b>Agreed Constructions</b>
substrate	C	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
transistor	C	<p>a three terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer, and the thin film transistor is formed using thin-film techniques on a substrate</p> <p><u>Intrinsic Support</u></p> <p>1:5-20; 1:44-46; 2:49-51; 3:21-63; 5:38-41; Figs 1-4; Abstract.</p>	<p>a three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate</p> <p><u>Intrinsic Support</u></p> <p>1:15-16; 4:26-31; Fig. 2; Fig. 3</p>	<p>Plain meaning or</p> <p>A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate</p> <p><u>Intrinsic Support</u></p> <p>4:23-31; 4:39-44; 6:55-61; Claim 4</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F**  
**LG DISPLAY USP 5,905,274**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
gate	L	<p>patterned electrically conductive material that includes a portion that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>1:5-39; 3:21-29; 3:41-64; 4:26-34; 4:40-5:7; 5:21-37; 5:63-6:7; 6:15-48; 7:7-52; Figs 1-4; Abstract.</p>	<p>A region of a transistor</p> <p><u>Intrinsic Support</u></p> <p>4:26-31; Fig. 2; Fig. 3</p>	<p>same as gate electrode; a patterned, electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.</p> <p><u>Intrinsic Support</u></p> <p>E.g., 4:26-5:3</p>
a double layered structure	C A	<p>a structure of an electrically conductive material that includes two sequentially deposited metal layers</p> <p><u>Intrinsic Support</u></p> <p>1:5-10; 1:20-43; 2:55-3:19; 3:27-64; 4:24-34; 4:40-62; 5:22-38; 5:42-62; 6:27-49; 7:32-52; Figs. 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment.</p>	<p>a structure having only two metal layers.</p> <p><u>Intrinsic Support</u></p> <p>1:17-23; 3:27-29; 4:32-34; 5:21-25; 6:27-29; Fig. 2; Fig. 3; Figs. 4A-F; Application, 08/918,119, Response, November 17, 1998</p>	<p>a two-layered step structure</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3-4; 1:20-2:65; 3:27-58; 4:23-59; 5:21-38; 6:27-48</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F**  
**LG DISPLAY USP 5,905,274**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
a second metal layer disposed on the first metal layer	L C	sequentially depositing the second metal layer above and in contact with the first metal layer  <u>Intrinsic Support</u>  1:20-27; 2:49-3:20; 3:27-40; 3:45-58; 4:26-39; 4:53-59; 5:21-38; 5:42-54; 7:32-59; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment.	The second metal layer is in contact with the first metal layer  <u>Intrinsic Support</u>  3:49-51; Abstract; Fig 3, Figs. 4A-F	a second metal layer precipitated above, supported by and in contact with the first metal layer  <u>Intrinsic Support</u>  E.g., 5:41-54
the first metal layer including aluminum	C	the first metal layer containing aluminum and possibly other materials  <u>Intrinsic Support</u>  1:6-10; 1:17-26; 1:40-43; 1:51-55; 3:22-26; 4:32-38; 5:42-54; 7:47-52, App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment.	Plain meaning	Plain meaning  <u>Intrinsic Support</u>  E.g., 4:34-36; 5:42-43; 1:17-22
the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer	C	the second metal layer is patterned to prevent hillock on the side surfaces of the first metal layer that are	the second metal layer prevents hillock on the sides of the aluminum first metal layer	the second metal layer being arranged on the first metal layer to prevent hillocks from forming on the side

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**LG DISPLAY USP 5,905,274**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
		<p>exposed to a subsequently deposited gate insulating layer</p> <p><u>Intrinsic Support</u></p> <p>1:17-43; 2:49-65; 3:21-29; 3:34-40; 5:21-38; 6:37-48; 7:47-52; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment.</p>	<p><u>Intrinsic Support</u></p> <p>1:20-38; 3:20-26; 6:40-47</p>	<p>portions of the aluminum first metal layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3-4; 1:20-2:65; 3:21-25; 4:46-55; 5:21-38; 6:27-48; App 08/918119, 11/17/98 Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance, page 2; App</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F**  
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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
				08/918462, 4/26/99 Office Action, pages, 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99, Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462, 4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9 10; App 09/983629, 8/8/01 Notice of Allowance, page 2
at the sides of the aluminum first metal layer	L C A	the side surfaces of the first metal layer that are exposed to a subsequently deposited gate insulating layer  <u>Intrinsic Support</u>  1:17-43; 2:49-65; 3:21-29; 3:34-40; 5:21-38; 6:37-48; 7:47-52; Figs 1-4; Abstract;	Indefinite	at the portions on the top surface of the first metal layer not covered by the second metal layer  <u>Intrinsic Support</u>  E.g., Figs. 3-4; 4:23-59; 5:21-38; 6:45-47 App 08/918119, 11/17/98

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
		App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment.		Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance; page 2; App 08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462,

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F**  
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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
				4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9 10; App 09/983629, 8/8/01 Notice of Allowance, page 2

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F**  
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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
the first metal layer being wider than the second metal layer by about 1 to 4 $\mu\text{m}$	L C A	<p>the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more than 1<math>\mu\text{m}</math> and less than 4<math>\mu\text{m}</math> greater than the width of the second metal layer</p> <p><u>Intrinsic Support</u></p> <p>1:51-2:21; 3:41-64; 4:32-52; 5:21-38; 5:55-62; 5:67-6:48; 7:47-52; Abstract; Figs. 1-4; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment.</p>	<p>The top surface of the first metal layer has a width that is about 1 to 4 <math>\mu\text{m}</math> wider than a width of the top surface of the second metal layer to form a double step. A double step is a structure where not all of the top surface of the first metal layer is covered by the second metal layer.</p> <p><u>Intrinsic Support</u></p> <p>1:23-2:65; 4:39-51; 5:25-37; 6:15-26; 6:40-47; Fig. 3; Figs 4A-F; Application, 918,119, Original Drawings; August 27, 1997; Application, 918,119, Request for Patent Drawing Revision, December 16, 1998, United Kingdom Application, 9804417.5, Office Action, May 21, 1998; United Kingdom Application, 9804417.5, Response, March 4, 1999</p>	<p>Indefinite; or the first metal layer is about 1 to 4 <math>\mu\text{m}</math> greater than the width of the second metal layer measured from a level defined by the top of the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>Figs. 3-4; 1:20-2:65; 4:23-59; 5:21-38; 5:57-6:7; 6:27-48; App 08/918119, 11/17/98 Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
				09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance, page 2; App 08/918462, 4/26/99 Office Action, pages, 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462, 4/13/00 Response, pages 4- 8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9 10; App 09/983629, 8/8/01 Notice of Allowance, page 2

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**LG DISPLAY USP 5,905,274**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
two side portions of the first metal layer having no second layer thereon	C	<p>the side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer</p> <p><u>Intrinsic Support</u></p> <p>2:5-26; 2:49-60; 3:21-29; 4:40-63; 5:21-38; 6:7-15; 6:27-49; 7:24-28; 7:47-52; Figs. 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment.</p>	<p>Plain meaning</p>	<p>the two side portions on the top surface of the first metal layer not covered by the second layer</p> <p><u>Intrinsic Support</u></p> <p>Figs. 3-4; 1:20-2:65; 4:23-59; 5:21-38; 5:57-6:7; 6:27-48 App 08/918119, 11/17/98 Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
				09/983629, 1/14/03 Notice of Allowance; page 2; App 08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462, 4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9-10; App 09/983629, 8/8/01 Notice of Allowance, page 2

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**LG DISPLAY USP 5,905,274**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
two side portions of the first metal layer having no second layer disposed thereon	C A	<p>the side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer</p> <p><u>Intrinsic Support</u>            2:5-26; 2:49-60; 3:21-29; 4:40-63; 5:21-38; 6:7-15; 6:27-49; 7:24-28; 7:47-52; Figs. 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment.</p>	<p>Plain meaning</p>	<p>The two side portions on the top surface of the first metal layer not covered by the second layer</p> <p><u>Intrinsic Support</u>            See above</p>

# **EXHIBIT G**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT G**  
**LG DISPLAY USP 6,815,321**

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
transistor	C	<p>A three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.</p> <p><u>Intrinsic Support</u></p> <p>1:20-40; 1:61-64; 2:64-68; 3:39-4:14; 5:56-58; Abstract.</p>	<p>A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate</p> <p>[The citations to the patent specification are to the column and line numbers in the grand-parent patent U.S. Patent No. 5,905,274.]</p> <p><u>Intrinsic Support</u></p> <p>1:15-15; 4:26-31; Fig. 2; Fig. 3</p>	<p>Plain meaning or</p> <p>A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate</p> <p><u>Intrinsic Support</u></p> <p>4:40-49; 4:57-62; 7:5-11</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
substrate	C	<p>the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support</p> <p><u>Intrinsic Support</u></p> <p>2:65-3:5; 3:59-4:10; 5:59-64; Figs 1-4; Abstract.</p>	<p>the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support</p>	Plain meaning
forming a second metal layer on the first metal layer	L C	<p>sequentially depositing the second metal layer above and in contact with the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>1:37-44; 2:65-3:37; 3:44-4:15; 4:44-56; 5:3-9; 5:39-55; 5:59-6:5; 7:47-67; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 4; App 09/243,556, 8/3/2001, Amendment; USP 6,340,610, Claims 1, 4.</p>	<p>The second metal layer is formed in direct contact with the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>3:49-51; Abstract; Fig. 3; Figs. 4A-F</p>	<p>forming a second metal layer above, supported by, and in contact with the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>Fig. 4; 5:59-6:5</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
depositing a second metal layer on the first metal layer	L C	<p>sequentially depositing the second metal layer above and in contact with the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>1:37-44; 2:65-3:37; 3:44-4:15; 4:44-56; 5:3-9; 5:39-55; 5:59-6:5; 7:47-67; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 4; App 09/243,556, 8/3/2001, Amendment; USP 6,340,610, Claims 1, 4.</p>	<p>The second metal layer is deposited in direct contact with the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>3:49-51; Abstract; Fig. 3; Figs. 4A-F</p>	<p>Precipitating a second metal layer above, supported by, and in contact with the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Fig. 4; 5:59-6:5</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
a double layered metal gate	C A	<p>a patterned structure of an electrically conductive material that includes two sequentially deposited metal layers and includes a portion that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>1:20-56; 1:37-60; 3:4-36; 3:39-4:14; 4:40-52; 4:57-5:24; 5:39-55; 5:59-6:25; 6:33-65; 7:23-67; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 4; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance; USP 6,548,829, Claim 1.</p>	<p>a double-layered metal gate is a gate having only two metal layers</p> <p><u>Intrinsic Support</u></p> <p>1:17-23; 3:27-29; 4:32-34; 5:21-25; 6:27-29; Fig. 2; Fig. 3; Figs. 4A-F; Application 08/918,119, Response, November 17, 1998</p>	<p>a gate electrode having a two-layered step structure</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3-4; 1:29-3:14; 3:44-4:9; 4:41-5:9; 5:38-55; 6:44-47; 6:58-62</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
gate	L	<p>patterned electrically conductive material that includes a portion that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>1:20-56; 1:37-60; 3:4-36; 3:39-4:14; 4:40-52; 4:57-5:24; 5:39-55; 5:59-6:25; 6:33-65; 7:23-67; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 4; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance; USP 6,548,829, Claim 1.</p>	<p>a region of a transistor</p> <p><u>Intrinsic Support</u></p> <p>4:26-31; Fig. 2; Fig. 3</p>	<p>same as gate electrode; a patterned, electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.</p> <p><u>Intrinsic Support</u></p> <p>E.g., 4:41-5:20</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 $\mu\text{m}$	L C A	<p>the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more than 1 <math>\mu\text{m}</math> and less than 4 <math>\mu\text{m}</math> greater than the width of the second metal layer</p> <p><u>Intrinsic Support</u></p> <p>2:1-39; 3:59-4:15; 4:50-5:2; 5:38-55; 6:5-13; 6:18-65; 7:40-43; 7:62-67; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 2, 4, 5; App 09/243,556, 9/6/2000, Office Action; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance; USP</p>	<p>The top surface of the first metal layer has a width that is about 1 to 4 <math>\mu\text{m}</math> wider than a width of the top surface of the second metal layer to form a double step. A double step is a structure where not all of the top surface of the first metal layer is covered by the second metal layer.</p> <p><u>Intrinsic Support</u></p> <p>1:23-2:65; 4:39-51; 5:25-37; 6:15-26; 6:40-47; Fig. 3; Figs 4A-F; Application, 918,119, Original Drawings; August 27, 1997; Application, 918,119, Request for Patent Drawing Revision, December 16, 1998, United Kingdom Application, 9804417.5, Office Action, May 21, 1998; United Kingdom Application, 9804417.5, Response, March 4, 1999</p>	<p>Indefinite; or the width of the first metal layer is about 1 to 4 <math>\mu\text{m}</math> greater than the width of the second metal layer when measured from a level defined by the top of the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Indefinite: Figs. 3-4; 2:29-3:14; 4:40-5:9; 5:38-55; 6:14-25; 6:45-54 App 08/918119, 11/17/98 Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
		6,340,610, Claim 1; USP 6,548,829, Claims 1 and 6.		Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance, page 2; App 08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462, 4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9-10; App 09/983629, 8/8/01 Notice of Allowance, page 2

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
first etching layer	L	the first metal layer  <u>Intrinsic Support</u>  Claims 1-22; See Specification Generally.	Indefinite	Indefinite
waking	L	making  <u>Intrinsic Support</u>  Claims 1-22; See Specification Generally; App 10/377,732, 3/4/2003, Application as filed; App 10/377,732, 5/27/2004, Terminal Disclaimer Transmittal.	Indefinite	Non-sensical; indefinite

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**LG DISPLAY USP 6,815,321**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
forming a single photoresist having a predetermined width on the second metal layer	C	<p>forming a pattern of single photosensitive material that has a specified width on the second metal layer</p> <p><u>Intrinsic Support</u></p> <p>1:40-60; 2:1-29; 2:65-36; 3:44-51; 3:66-4:9; 4:50-56; 5:58-6:44; 7:23-67; Figs. 1-4; Abstract; App 09/243,556, 9/6/2000, Office Action; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; USP 6,340,610 Claims 1, 2.</p>	<p>The photoresist is deposited in direct contact with the second metal layer</p> <p><u>Intrinsic Support</u></p> <p>3:41-58; 6:15-18; Figs. 4A-F</p>	Plain meaning
photoresist	C	<p>pattern of a photosensitive material</p> <p><u>Intrinsic Support</u></p> <p>1:40-60; 2:1-29; 2:65-36; 3:44-51; 3:66-4:9; 4:50-56; 5:58-6:44; 7:23-67; Figs. 1-4; Abstract.</p>	<p>An etching mask</p> <p><u>Intrinsic Support</u></p> <p>3:41-58; 6:15-18; Figs. 4A-F</p>	Plain meaning

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT G**  
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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
simultaneously in a single etching step using the single photoresist as a mask	L	during a single etching process with a common mask	The first and second metal layers are simultaneously etched in a single step using the photoresist as a mask	<p>construe term:  "patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask"</p> <p>as</p> <p>forming the patterned first and second metal layers in one chemical etching step using one photoresist mask</p> <p><u>Intrinsic Support</u></p> <p>1:40-60; 2:1-29; 2:65-36; 3:44-51; 3:66-4:9; 4:50-56; 5:58-6:44; 7:23-67; Abstract; App 09/243,556, 9/6/2000, Office Action; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; USP 6,340,610, Claims 1, 2.</p> <p><u>Intrinsic Support</u></p> <p>5:55-62; 7:15-30</p> <p><u>Intrinsic Support</u></p> <p>E.g., Fig. 4; 5:39-43; 6:6-12</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT G**  
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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
simultaneously patterning/patterning . . . simultaneously	A	<p>removing part of the first and second metal layers during a single etching process</p> <p><u>Intrinsic Support:</u></p> <p>Abstract; 1:40-60; 2:1-29; 2:65-36; 3:44-51; 3:66-4:9; 4:50-56; 5:58-6:44; 7:23-67; Figs. 1, 4; USP 6,340,610, Claims 1, 2; App 09/243,556, 9/6/2000 Office Action; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001 Amendment.</p>	Plain meaning	<p>Forming the patterned first and second metal layers at the same time in one chemical etching step</p> <p><u>Intrinsic Support</u></p> <p>E.g., Fig. 4; 5:39-43; 6:6-12; App 08/918119, 11/17/98 Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance, page 2; App</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
				08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462, 4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages, 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9 10; App 09/983629, 8/8/01 Notice of Allowance, page 2

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT G**  
**LG DISPLAY USP 6,815,321**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
the first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4 $\mu\text{m}$	L C A	<p>the first and second metal layers are etched such that the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more than 1 <math>\mu\text{m}</math> and less than 4 <math>\mu\text{m}</math> greater than the width of the second metal layer</p> <p><u>Intrinsic Support</u></p> <p>2:1-39; 3:59-4:15; 4:50-5:2; 5:38-55; 6:5-13; 6:18-65; 7:40-43; 7:62-67; Figs. 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274 Claims 1, 2, 4, 5; App 09/243,556, 9/6/2000, Office Action; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App</p>	<p>The first metal layer being etched so that a top surface of the first metal layer has a width that is about 1 to 4 <math>\mu\text{m}</math> wider than a width of the top surface of the second metal layer to form a double step. A double step is a structure where not all of the top surface of the first metal layer is covered by the second metal layer.</p> <p><u>Intrinsic Support</u></p> <p>1:23-2:65; 4:39-51; 5:25-37; 6:15-26; 6:40-47; Fig. 3; Figs 4A-F; Application, 918,119, Original Drawings; August 27, 1997; Application, 918,119, Request for Patent Drawing Revision, December 16, 1998, United Kingdom Application, 9804417.5, Office Action, May 21, 1998; United Kingdom Application, 9804417.5, Response, March 4, 1999</p>	<p>indefinite;</p> <p>or</p> <p>the first metal layers being etched so that the width of the first metal layer is about 1 to 4 <math>\mu\text{m}</math> greater than the width of the second metal layer when measured from a level defined by the top of the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Indefinite: Figs. 3-4; 2:29-3:14; 4:40-5:9; 5:38-55; 6:14-25; 6:45-54 App 08/918119, 11/17/98 Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
		09/243,556, 9/10/2001, Notice of Allowance; USP 6,340,610, Claim 1; USP 6,548,829, Claims 1 and 6.		Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance, page 2; App 08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462, 4/13/00 Response, pages 4- 8; App 08/918462, 07/7/00 Office Action, pages, 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9 10; App 09/983629, 3/8/01

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT G**  
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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
a first and a second side portion being exposed from the second metal layer	C	<p>first and second side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer</p> <p><u>Intrinsic Support</u></p> <p>1:34-60; 2:65-3:14; 3:39-47; 3:52-57; 5:38-55; 6:55-65; 7:62-67; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 2, 4, 5; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance.</p>	Plain meaning	<p>Notice of Allowance, page 2</p> <p>A first side portion and a second side portion on the top surface of the first metal layer not covered by the second layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Indefinite: Figs. 3-4; 4:40-5:9; 5:38-55; 6:45-54; 6:58-62 App 08/918119, 11/17/98 Response, pages 3-4.; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action,</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
				pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance, page 2; App 08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462, 4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9-10; App 09/983629, 8/8/01 Notice of Allowance, page 2

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
two side portions of the first metal layer having no second metal layer deposited thereon	C A	<p>the side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer</p> <p><u>Intrinsic Support</u></p> <p>1:34-60; 2:65-3:14; 3:39-47; 3:52-57; 5:38-55; 6:55-65; 7:62-67; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 2, 4, 5; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance</p>	Plan meaning	<p>The two portions on the top surface of the first metal layer not covered by the second metal layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Indefinite: Figs. 3-4; 4:40-5:9; 5:38-55; 6:45-54; 6:58-62 App 08/918119, 11/17/98 Response, pages 3-4,; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
				11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance, page 2; App 08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462, 4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9-10; App 09/983629, 8/8/01 Notice of Allowance, page 2

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
the first metal layer including aluminum	C	<p>the first metal layer containing aluminum and possibly other materials</p> <p><u>Intrinsic Support</u></p> <p>1:20-28; 1:34-44; 1:56-60; 2:1-5; 3:39-44; 4:50-56; 5:59-6:5; 7:62-67; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 4; App 09/243,556, 3/11/1999, Preliminary Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment.</p>	<p>A first metal layer that includes pure aluminum</p> <p><u>Intrinsic Support</u></p> <p>4:34-36; 5:41-42</p>	Plain meaning

# **EXHIBIT H**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT H**  
**LG DISPLAY USP 7,176,489**

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
transistor	C	A three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.	A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate	Plain meaning  or  A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
substrate	C	<p>the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support</p> <p><u>Intrinsic Support:</u></p> <p>2:64-3:3; 3:59-4:8; 5:59-64; Figs 1-4; Abstract.</p>	<p>the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support</p>	<p>Plain meaning; or The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
a double layered metal gate	C A	<p>a patterned structure of an electrically conductive material that includes two sequentially deposited metal layers and includes a portion that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>1:21-56; 1:38-60; 3:4-34; 3:39-4:13; 4:41-53; 4:58-5:25; 5:39-55; 5:59-6:25; 6:33-65; 7:24-8:26; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 4; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance; USP 6,548,829, Claim 1.</p>	<p>a gate having only two metal layers</p> <p><u>Intrinsic Support</u></p> <p>1:17-23; 3:27-29; 4:32-34; 5:21-25; 6:27-29; Fig. 2; Fig. 3; Figs. 4A-F; Application, 08/918,119, Response, November 17, 1998</p>	<p>A gate electrode having a two-layered step structure</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3-4; 1:29-3:14; 3:44-4:9; 4:41-5:9; 5:38-55; 6:44-47; 6:58-62</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
gate	L	<p>patterned electrically conductive material that includes a portion that controls current flow through the channel between the source electrode and drain electrode</p> <p><u>Intrinsic Support</u></p> <p>1:21-56; 1:38-60; 3:3-35; 3:39-4:13; 4:41-53; 4:58-5:25; 5:39-55; 5:59-6:25; 6:33-65; 7:24-8:26; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 4; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance; USP 6,548,829, Claim 1.</p>	<p>a region of a transistor</p> <p><u>Intrinsic Support</u></p> <p>4:26-31; Fig. 2; Fig. 3</p>	<p>same as gate electrode; a patterned electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode</p> <p><u>Intrinsic Support</u></p> <p>E.g., 3:44-50; 4:41-5:21</p>

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<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
having a first metal layer and a second metal layer thereon	L C	<p>sequentially depositing the second metal layer above and in contact with the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>1:38-44; 2:64-3:37; 3:44-4:13; 4:44-57; 5:4-10; 5:39-55; 5:59-6:5; 8:6-26; Figs 1-4; Abstract; App 8/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 4; App 09/243,556, 8/3/2001, Amendment; USP 6,340,610, Claims 1, 4.</p>	<p>the second metal layer is in contact with the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>3:49-51; Abstract; Fig. 3; Figs. 4A-F</p>	<p>The double layered metal gate having a first metal layer and a second metal layer formed on the top surface of the first metal layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3-4; 5:59-6:5</p>
a total width of the first metal layer being greater than a total width of the second metal layer by about 1 to 4 $\mu\mu$	L C A	<p>the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more than 1<math>\mu\mu</math> and less than 4<math>\mu\mu</math> greater than the width of the second metal layer</p>	<p>The top surface of the first metal layer has a width that is about 1 to 4 <math>\mu\mu</math> wider than a width of the top surface of the second metal layer to form a double step. A double step is a gate where not all of the top surface of the first metal layer is covered by the second metal layer.</p>	<p>Indefinite; or The width of the first metal layer is about 1 to 4 <math>\mu\mu</math> greater than the width of the second metal measured from a level defined by the top of the first metal layer</p>

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Claim Terms	Des.	LGD Construction	CMO Construction	AUO Construction
		<p><u>Intrinsic Support</u></p> <p>2:1-38; 3:58-4:13; 4:51-5:3; 5:39-55; 6:6-13; 6:18-65; 7:41-8:2; 8:21-26; Figs. 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 2, 4, 5; App 09/243,556, 9/6/2000, Office Action; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance; USP 6,340,610, Claim 1; USP 6,548,829, Claims 1 and 6.</p>	<p><u>Intrinsic Support</u></p> <p>1:23-2:65; 4:39-51; 5:25-37; 6:15-26; 6:40-47; Fig. 3; Figs 4A-F; Application, 918,119, Original Drawings; August 27, 1997; Application, 918,119, Request for Patent Drawing Revision, December 16, 1998, United Kingdom Application, 9804417.5, Office Action, May 21, 1998; United Kingdom Application, 9804417.5, Response, March 4, 1999</p>	<p><u>Intrinsic Support</u></p> <p>Indefinite: Figs. 3-4; 2:29-3:14; 4:40-5:9; 5:38-55; 6:14-25; 6:45-54;</p> <p>App 08/918119, 11/17/98 Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT H**  
**LG DISPLAY USP 7,176,489**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
				Notice of Allowance, page 2; App 08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6 ; App 08/918462, 4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9 10; App 09/983629, 8/8/01 Notice of Allowance, page 2
a first and second side portion being exposed from the second metal layer	C A	first and second side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer	Plain meaning	The two side portions on the top surface of the first metal layer not covered by the second metal layer

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT H**  
**LG DISPLAY USP 7,176,489**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
		<u>Intrinsic Support</u>  1:35-60; 2:64-3:13; 3:39-46; 3:51-57; 5:39-55; 6:55-65; 8:21-26-; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 2, 4, 5; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance.		<u>Intrinsic Support</u>  E.g., Figs. 3-4; 4:40-5:9; 5:38-55; 6:45-55; 6:58-63; App 08/918119, 11/17/98 Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages, 2-5; App 09/243556, 8/3/91 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance, page 2; App 08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT H**  
**LG DISPLAY USP 7,176,489**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
				1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action, pages 3-6; App 08/918462, 4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9-10; App 09/983629, 8/8/01 Notice of Allowance, page 2
side portion of the first metal layer	A	<p>side surface of the first metal layer exposed to the subsequently deposited gate insulating layer</p> <p><u>Intrinsic Support</u></p> <p>1:35-60; 2:64-3:13; 3:39-50; 3:51-57; 5:39-55; 6:55-65;</p>	<p>Plain meaning</p>	<p><i>Construed with "each" in front:</i></p> <p>Each of the first and second side portions on the top surface of the first metal layer not covered by the second metal layer</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3-4; 4:40-5:9; 5:38-55; 6:45-55 6:58-62;</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT H**  
**LG DISPLAY USP 7,176,489**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
		8:21-26; Figs 1-4; Abstract; App 08/918,119, 8/20/1998, Office Action; App 08/918,119, 11/25/1998, Amendment; USP 5,905,274, Claims 1, 2, 4, 5; App 09/243,556, 1/8/2001, Amendment; App 09/243,556, 3/29/2001, Office Action; App 09/243,556, 8/3/2001, Amendment; App 09/243,556, 9/10/2001, Notice of Allowance.		App 08/918119, 11/17/98 Response, pages 3-4; App 10/377,732, 2/27/04 Office Action, pages 2-5; App 10/377,732, 5/27/04 Terminal Disclaimer, pages 1-2; App 10/872,527, 9/30/05 Office Action, pages 2-3; App 10/872,527, 3/29/06 Office Action, page 2; App 10/872,527, 8/29/06 Response, page 2; App 09/243556, 1/8/01 Response, page 7; App 09/243556, 3/29/01 Office Action, pages 2-5; App 09/243556, 8/3/01 Response, pages 4-7; App 09/983629, 8/14/02 Office Action, pages 4-11; App 09/983629, 11/13/02 Office Action, pages 5-6; App 09/983629, 1/14/03 Notice of Allowance, page 2; App 08/918462, 4/26/99 Office Action, pages 1-2; App 08/918462, 9/10/99 Interview Summary, pages 1-2; App 08/918462, 9/27/99 Response, Remark Section; App 08/918462, 12/14/99 Office Action,

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT H**  
**LG DISPLAY USP 7,176,489**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
				pages 3-6; App 08/918462, 4/13/00 Response, pages 4-8; App 08/918462, 07/7/00 Office Action, pages 2-5; App 08/918462, 11/7/00 Response, pages 4-10; App 08/918462, 12/5/00 Interview Summary; App 08/918462, 1/23/01 Office Action, pages 2-4; App 08/918462, 4/4/01 Response, pages 4-7 and 9-10; App 09/983629, 8/8/01 Notice of Allowance, page 2

# **EXHIBIT I**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT I**  
**LG DISPLAY USP 7,218,374**

<b>Claim Terms</b>	<b>Des.</b>	<b>Agreed Constructions</b>
UV sealant	C	sealant material that is at least partially curable by UV light
forming a main UV sealant	L	The combination of the construction for “forming a main sealant” with the agreed construction of “UV sealant”
auxiliary UV sealant	C A	The combination of the construction for “auxiliary sealant” with the agreed construction of “UV sealant”
main UV sealant	C A	The combination of the construction for “main sealant” with the agreed construction of “UV sealant”

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
preparing a lower substrate and an upper substrate	C	making the substrates ready for depositing sealant and liquid crystal material prior to attachment  <u>Intrinsic Support</u>  4:30-67; Fig. 3A.	Indefinite	Indefinite  <u>Intrinsic Support</u>  E.g., Figs. 3, 4, 5, & 6; 4:23-67; 6:40-67; 7:27-58; 7:64-34
forming a main sealant	L	depositing sealant material that encloses the display region  <u>Intrinsic Support</u>  2:36-40; 3:20-25, 5:5-7; Figs. 2B, 3B, 4A, and 5A.	forming sealant material necessary for confining liquid crystal from leaking out from between the substrates  <u>Intrinsic Support</u>  Abstract; 3:20-24; 3:35-41; 3:55-4:11; 5:3-30; 6:34-39;	forming a segment of sealant that encloses the liquid crystal in the LCD panel  <u>Intrinsic Support</u>  E.g., Figs. 3, 4, 5, & 6; 3:9-40; 5:1-64; 6:40-67 App 10/184118, 12/1/03 OA,

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT I**  
**LG DISPLAY USP 7,218,374**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
			7:11-16; 7:63-8:2; Figs. 1A-1D, 2A-2C, 3A-3D, 4A-4D, 5A-5B, 6	pages 2-7; App 10/184118, 2/4/04 Amendment in Response to Non-Final Office Action, pages 7-9; App 10/184118, 04/26/2004, pages 2-7; App 10/184118, 7/15/2004 Reply Under 37 C.F.R. Section 1.111, pages 2-6 App 10/184118, 11/18/2004 OA, pages 2-8; App 10/184118, 02/16/2005 Response after Office Action, pages 2-7; App 10/184118, 04/18/2005 Response as Submission under 37 C.F.R. 1.114, pages 6-11; App 10/184118, 06/15/2005 Office Action, pages 2-4; App 10/184118, 09/15/2005 Response to non-final Office Action, pages 6-7; App 10/184118, 12/01/2005 Office Action, pages 2-4; App 10/184118, 03/01/2006 Response to Final Office Action, pages 7; App 10/184118, 06/19/2006 Office Action, pages 2-8; App 10/184118, 09/15/2006 Response to Non-final Office Action, page 5; App 10/184118,

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT I**  
**LG DISPLAY USP 7,218,374**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
				10/11/2006 Notice of Allowability, page 2.
main sealant	C A	sealant material that encloses the display region  <u>Intrinsic Support</u>  2:36-40; 3:20-25, 5:5-20; 7:63-8:2; Figs. 2B, 3B, 4A, and 5A.	sealant material necessary for confining liquid crystal from leaking out from between the substrates  <u>Intrinsic Support</u>  Abstract; 3:20-24; 3:35-41; 3:55-4:11; 5:3-30; 6:34-39; 7:11-16; 7:63-8:2; Figs. 1A-1D, 2A-2C, 3A-3D, 4A-4D, 5A-5B, 6	A segment of sealant for enclosing the liquid crystal in the LCD panel  <u>Intrinsic Support</u>  See above
auxiliary sealant	C A	sealant deposited in an area outside of the main sealant  <u>Intrinsic Support</u>  5:7-20; 7:63-8:2; Figs. 3B, 4A, and 5A.	sealant material that is not necessary for confining liquid crystal from leaking out from between the substrates  <u>Intrinsic Support</u>  Abstract; 1:20-23; 3:20-24; 3:35-41; 3:55-4:11; 5:3-20; 6:34-39; 7:11-16; 7:63-8:2; Figs. 1A-1D, 2A-2C, 3A-3D, 4A-4D, 5A-5B, 6	A segment of sealant for that extends from the main sealant and is outside the enclosure of the main sealant  <u>Intrinsic Support</u>  E.g., Fig. 4, 5, & 6; 3:9-40; 5:1-64; 6:40-67

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT I**  
**LG DISPLAY USP 7,218,374**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
a dummy region	L A	<p>an area outside of the main sealant</p> <p><u>Intrinsic Support</u></p> <p>5:7-20; 7:63-8:2; Figs. 3B, 4A, and 5A.</p>	<p>an area outside the boundary of the main sealant</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:20-23; 2:5-55; 3:9-40; 3:55-4:11; 5:3-20; 5:27-51; 6:34-39; 7:63-8:2; 8:14-17; Figs. 1A-1D, 2A-2C, 3A-3D, 4A-4D, 5A-5B, 6; App. 10/184,118, 11/18/04 Office Action, page 2-3; 2/16/05 Amendment at page 2</p>	<p>An area outside the , enclosure of the main sealant</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 2, 3, 4, 5, &amp; 6; 2:47-54; 3:9-40; 5:1-64; 6:40-67</p>
connects to the main sealant	L	<p>joined to the main sealant</p> <p><u>Intrinsic Support</u></p> <p>2:41-55; 5:7-20; 7:63-8:2; Figs. 3B, 4A, and 5A; App 10/184,118, 7/16/04, Response, pagse 2; App 10/184,118, 2/16/05 Response, pages 2-3; App 10/184,118, 4/18/05 Response, pages 6-7; App 10/184,118, 11/27/06 Response, page 2.</p>	<p>physically attached to the main sealant</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:20-23; 2:5-55; 3:9-40; 3:55-4:11; 5:3-20; 5:27-51; 6:34-39; 7:63-8:2; 8:14-17; Figs. 1A-1D, 2A-2C, 3A-3D, 4A-4D, 5A-5B, 6; App. 10/184,118, 11/18/04 Office Action, page 2-3; 2/16/05 Amendment at page 2</p>	<p>Physically attached to the main sealant</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, 5, &amp; 6; 5:1-64; 6:40-67</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT I**  
**LG DISPLAY USP 7,218,374**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
wherein the auxiliary UV sealant is formed in a dummy region and extends outside from the main UV sealant	L C A	<p>wherein the auxiliary UV sealant is deposited in an area that is outside of the main UV sealant and is joined to the main UV sealant</p> <p><u>Intrinsic Support</u></p> <p>2:41-55; 5:7-20; 7:63-8:2; Figs. 3B, 4A, and 5A; App 10/184,118, 7/16/04, Response, page 2; App 10/184,118, 2/16/05 Response, pages 2-3; App 10/184,118, 4/18/05 Response, pages 6-7 App 10/184,118, 11/27/06 Response, page 2.</p>	<p>wherein the auxiliary UV sealant is formed in an area outside the boundary of the main UV sealant beginning from the main UV sealant and moving outward</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:20-23; 2:5-55; 3:9-40; 3:55-4:11; 5:3-20; 5:27-51; 6:34-39; 7:63-8:2; 8:14-17; Figs. 1A-1D, 2A-2C, 3A-3D, 4A-4D, 5A-5B, 6; App. 10/184,118, 3/1/06 Response, pages 5, 7</p>	<p>Wherein the auxiliary UV sealant is formed in an area outside the enclosure of the main UV sealant</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, 5, &amp; 6; 5:1-6:9; 6:40-67</p>
wherein the auxiliary sealant and the main sealant are contiguous	L C A	<p>wherein the auxiliary and main sealants are deposited in a continuous process</p> <p><u>Intrinsic Support</u></p> <p>2:41-55; 5:7-20; 7:63-8:2; Figs. 3B, 4A, and 5A; App 10/184,118, 7/16/04, Response, page 2; App 10/184,118, 2/16/05 Response, pages 2-3; App</p>	<p>wherein the auxiliary sealant touches but does not overlap the main sealant</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:20-23; 2:5-55; 3:9-40; 3:55-4:11; 5:3-20; 5:27-51; 6:34-39; 7:63-8:2; 8:14-17; Figs. 1A-1D, 2A-2C, 3A-3D, 4A-4D, 5A-5B, 6; App. 10/184,118, 6/19/06</p>	<p>Wherein the auxiliary sealant and the main sealant are physically connected to each other</p> <p><u>Intrinsic Support</u></p> <p>E.g., Figs. 3, 4, 5, &amp; 6; 5:1-6:4; 6:40-67 App 10/184118, 12/1/03 OA, pages 2-7; App 10/184118, 2/4/04 Amendment in Response to Non-Final Office Action,</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT I**  
**LG DISPLAY USP 7,218,374**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
		10/184,118, 4/18/05 Response, pages 6-7; App 10/184,118, 11/27/06 Response, page 2.	Office Action, page 3, 4; 9/15/06 Amendment, page 2, 5	pages 7-9; App 10/184118, 04/26/2004, pages 2-7; App 10/184118, 7/15/2004 Reply Under 37 C.F.R. Section 1.111, pages 2-6 App 10/184118, 11/18/2004 OA, pages 2-8; App 10/184118, 02/16/2005 Response after Office Action, pages 2-7; App 10/184118, 04/18/2005 Response as Submission under 37 C.F.R. 1.114, pages 6-11; App 10/184118, 06/15/2005 Office Action, pages 2-4; App 10/184118, 09/15/2005 Response to non-final Office Action, pages 6-7; App 10/184118, 12/01/2005 Office Action, pages 2-4; App 10/184118, 03/01/2006 Response to Final Office Action, pages 7; App 10/184118, 06/19/2006 Office Action, pages 2-8; App 10/184118, 09/15/2006 Response to Non-final Office Action, page 5; App 10/184118, 10/11/2006 Notice of Allowability, page 2

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT I**  
**LG DISPLAY USP 7,218,374**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
wherein the auxiliary UV sealant contacts the main UV sealant	C A	wherein the auxiliary UV sealant touches the main UV sealant  <u>Intrinsic Support</u>  2:41-55; 5:7-20; 7:63-8:2; Figs. 3B, 4A, and 5A; App 10/184,118, 7/16/04, Response, page 2; App 10/184,118, 2/16/05 Response, pages 2-3; App 10/184,118, 4/18/05 Response, pages 6-7; App 10/184,118, 11/27/06 Response, page 2.	wherein the auxiliary UV sealant touches the main UV sealant  <u>Intrinsic Support</u>  Abstract; 1:20-23; 2:5-55; 3:9-40; 3:55-4:11; 5:3-20; 5:27-51; 6:34-39; 7:63-8:2; 8:14-17; Figs. 1A-1D, 2A-2C, 3A-3D, 4A-4D, 5A-5B, 6; App. 10/184,118, 6/19/06 Office Action, page 3, 4; 9/15/06 Amendment, page 4, 5	wherein the auxiliary sealant and the main sealant are physically connected together  <u>Intrinsic Support</u>  E.g., Figs. 3, 4, 5, & 6; 5:1-6:9; 6:40-67
applying a liquid crystal on one of the lower and upper substrates	L C A	depositing the liquid crystal onto either one of the substrates  <u>Intrinsic Support</u>  5:65 - 6:9; Fig. 3B.	plain meaning  <u>Intrinsic Support</u>  Abstract; 1:31-55; 2:5-15; 2:34-40; 3:25-34; 5:27-5:51; Figs. 1A-1D; 3A-3D	Plain meaning  <u>Intrinsic Support</u>  E.g., Figs. 3, 4, 5, & 6; 5:65-6:9; 6:40-67 App 10/184118, 12/1/03 OA, pages 2-7; App 10/184118, 2/4/04 Amendment in Response to Non-Final Office Action, pages 7-9; App 10/184118, 04/26/2004, pages 2-7; App

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT I**  
**LG DISPLAY USP 7,218,374**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
				10/184118, 7/15/2004 Reply Under 37 C.F.R. Section 1.111, pages 2-6 App 10/184118, 11/18/2004 OA, pages 2-8; App 10/184118, 02/16/2005 Response after Office Action, pages 2-7; App 10/184118, 04/18/2005 Response as Submission under 37 C.F.R. 1.114, pages 6-11; App 10/184118, 06/15/2005 Office Action, pages 2-4; App 10/184118, 09/15/2005 Response to non-final Office Action, pages 6-7; App 10/184118, 12/01/2005 Office Action, pages 2-4; App 10/184118, 03/01/2006 Response to Final Office Action, pages 7; App 10/184118, 06/19/2006 Office Action, pages 2-8; App 10/184118, 09/15/2006 Response to Non-final Office Action, page 5; App 10/184118, 10/11/2006 Notice of Allowability, page 2

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT I**  
**LG DISPLAY USP 7,218,374**

<b>Claim Terms</b>	<b>Des.</b>	<b>LGD Construction</b>	<b>CMO Construction</b>	<b>AUO Construction</b>
attaching the lower and upper substrates	A	pressing the lower and upper substrates together  <u>Intrinsic Support</u>  6:4-6; Figs. 1C and 2C.	putting the lower and upper substrates together as one single piece  <u>Intrinsic Support</u>  Abstract; 1:27-28; 3:25-34; 5:65-6:15; Figs. 1A-1D; 3A 3D	Putting the lower and upper substrates together as one single piece  <u>Intrinsic Support</u>  E.g., Figs. 3, 4, 5, & 6; 5:65-6:9; 6:40-67

# **EXHIBIT J**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT J**  
**AU Optronics USP 5,748,266**

<b>Claim Terms</b>	<b>Des.</b>	<b>Agreed Constructions</b>
color filter	L	A filter that modifies light from a source so as to allow one or more selected colors to pass through to the viewer side of the display. A color filter is formed on the color filter substrate.
color filter substrate	A	the structure on which the color filter is formed that faces the TFT substrate
active element	A	an element that controls voltage or current, typically one or more transistors located at each pixel location

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
common electrode	L	<p>a conductor, typically made of a transparent material, on the color filter substrate that receives a reference voltage relative to which the pixel electrode voltages can be measured</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:57-60, Figs. 1 and 2; 2:1-12; 2:25-3:29, esp. 2:29-42, and Figs. 3 and 4; 3:35-38, and Fig. 2; 4:65-5:44, esp. 4:67-5:6, and Fig 8; 6:26-43, 6:47-51, and Figs. 6-11, esp. element 30; 6:52-7:32, esp. 7:8-19; 8:24-25; claims 1, 3, 6, and 7.</p>	<p>a conductor, typically made of a transparent material, on the color filter substrate that receives a reference voltage relative to the pixel electrode voltages</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:57-2:04; 2:25-42; 2:43-3:65; 5:07-10; 7:09-14; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT J**  
**AU Optronics USP 5,748,266**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
pillars formed higher than other portions of the color filter	L	<p>the pillars are formed higher than the highest portions of the color filter.</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 4:65-5:6, and Fig. 8; 5:57-6:5; 6:26-43, 6:47-51, and Figs. 6-11, esp. elements 78 and 32; 7:4-31, and Fig. 8; 8:20-23; claims 1-5, 7, 9 and 10; March 5, 1997 Office Action, esp. at 2-3; July 7, 1997 Response, esp. at 6-7.</p>	<p>patterned structures of the color filter that protrude toward the pixel array beyond the height of non-pillar portions of the color filter substrate to act as a spacer</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:13-19; 3:66-4:21; 4:21-30; 4:31-49; 4:51-64; 4:65-5:06; 5:07-10; 5:57-6:05; 7:09-14; 7:32-43; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11; JP H08-262484 at paragraphs [0017]-[0032]; App 08/615,012, 7/7/1997 Amendment, pages 2-7.</p>
objects formed on the array substrate	L	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 4:65-5:6, and Fig. 8; 5:57-6:5; 6:26-43, 6:47-51, and Figs. 6-11; 7:4-31, and Fig. 8; 8:28-34; claims 1, 3, 6 and 7. March 5, 1997 Office Action, esp. at 2-3; July 7, 1997 Response, esp. at 6-7.</p>	<p>structures having one or more patterned layers in the pixel array</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:13-19; 3:66-4:21; 4:21-30; 4:31-49; 4:51-64; 4:65-5:06; 5:07-10; 5:57-6:05; 7:09-14; 7:32-43; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11; JP H08-262484 at paragraphs [0017]-[0032]; App 08/615,012, 7/7/1997 Amendment, pages 2-7.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT J**  
**AU Optronics USP 5,748,266**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
the pillars are covered with the common electrode	L	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 4:65-5:6, and Fig. 8; 6:26-43, 6:47-51, and Figs. 6-11, esp. elements 78 and 30; 7:4-13, and Fig. 8; 8:24-25; 8:28-34; claims 1, 3 and 7; March 5, 1997 Office Action, esp. at 2-3; July 7, 1997 Response, esp. at 6-7.</p>	<p>the common electrode is formed to cover the protruded surface of the pillars</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:57-2:04; 2:13-19; 2:25-42; 2:43-3:65; 3:66-4:21; 4:21-30; 4:31-49; 4:51-64; 4:65-5:06; 5:07-10; 5:57-6:05; 7:09-14; 7:32-43; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11; JP H08-262484 at paragraphs [0017]-[0032]; App 08/615,012, 7/7/1997 Amendment, pages 2-7.</p>
pillars being formed higher than other portions of the facing substrate	L	<p>the pillars are formed higher than the highest portions of the color filter substrate.</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 4:65-5:6, and Fig. 8; 5:57-6:5; 6:26-43, 6:47-51, and Figs. 6-11, esp. elements 78 and 32; 7:4-31, and Fig. 8; 8:20-23; claims 1-5, 7, 9 and 10; March 5, 1997 Office Action, esp. at 2-3; July 7, 1997 Response, esp. at 6-7.</p>	<p>patterned structures that protrude toward the pixel array beyond the height of non-pillar portions of the color filter substrate to act as a spacer</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:13-19; 3:66-4:21; 4:21-30; 4:31-49; 4:51-64; 4:65-5:06; 5:07-10; 5:57-6:05; 7:09-14; 7:32-43; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11; JP H08-262484 at paragraphs [0017]-[0032]; App 08/615,012, 7/7/1997 Amendment, pages 2-7.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT J**  
**AU Optronics USP 5,748,266**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
common electrode for all pixels covering at least some of the pillars	L	<p>Plain meaning:</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 4:65-5:6, and Fig. 8; 6:26-43, 6:47-51, and Figs. 6-11, esp. elements 78 and 30; 7:4-13, and Fig. 8; 8:24-25; 8:28-34; claims 1, 3 and 7; March 5, 1997 Office Action, esp. at 2-3; July 7, 1997 Response, esp. at 6-7.</p>	<p>the common electrode is formed on the protruded surface of at least some of the pillars</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:57-2:04; 2:25-42; 2:43-3:65; 4:31-49; 4:51-64; 4:65-5:06; 5:07-10; 5:57-6:05; 7:09-14; 7:32-43; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11; JP H08-262484 at paragraphs [0017]-[0032]; App 08/615,012, 7/7/1997 Amendment, pages 2-7.</p>
the common electrode being electrically connected to the storage capacitance line at the portions of the common electrode covering the pillars	L	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 4:65-5:44, and Fig. 8; 6:26-43, 6:47-51, and Figs. 6-11; 7:4-43, and Fig. 8; 8:24-25; 8:28-34; claims 1, 3 and 7; March 5, 1997 Office Action, esp. at 2-3; July 7, 1997 Response, esp. at 6-7.</p>	<p>the common electrode is electrically connected to the storage capacitance line in the pixel area where the pillars covered with the common electrode contact the objects on the array substrate</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:45-48; 1:57-2:04; 2:13-19; 2:25-42; 2:43-3:65; 4:31-49; 4:51-64; 4:65-5:06; 5:07-10; 5:57-6:05; 7:09-14; 7:32-43; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11; JP H08-262484 at paragraphs [0017]-[0032]; App 08/615,012, 7/7/1997 Amendment, pages 2-7.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT J**  
**AU Optronics USP 5,748,266**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
storage capacitance line for outputting the reference potential of the storage capacitance	L	<p>the storage capacitance line is connected to the capacitor(s), and therefore outputs the reference potential of the storage capacitance</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:45-48, and Figs. 1 and 2; 2:31-40, and Figs. 3 and 4; 4:65-5:44, and Fig. 8; 6:26-43, 6:47-51, and Figs. 6-11, esp. element 28; claims 3, 6, 7, and 9; March 5, 1997 Office Action, esp. at 2-3; July 7, 1997 Response, esp. at 6-7.</p>	<p>a pattern of electrically conductive material within the pixel area for providing a reference voltage to the storage capacitors</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:45-48; 1:57-2:04; 2:25-42; 2:43-3:65; 4:31-49; 4:65-5:06; 5:07-10; 7:09-14; 7:32-43; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11; JP H08-262484 at paragraphs [0017]-[0032]; App 08/615,012, 7/7/1997 Amendment, pages 2-7.</p>
storage capacitance line	A	<p>a line or wire of conductive material, typically metal, connected to one or more storage capacitors of the TFT array</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:45-48, and Figs. 1 and 2; 2:31-40, and Figs. 3-4; 4:67-5:44, esp. 5:14-18, and Fig. 8; 6:26-43, 6:47-51, and Figs. 6-11, esp. element 28; claims 3, 6, 7, and 9; March 5, 1997 Office Action, esp. at 2-3; July 7, 1997 Response, esp. at 6-7.</p>	<p>a pattern of electrically conductive material within the pixel area for providing a reference voltage to the storage capacitors</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:45-48; 1:57-2:04; 2:25-42; 2:43-3:65; 4:31-49; 4:65-5:06; 5:07-10; 7:09-14; 7:32-43; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11; JP H08-262484 at paragraphs [0017]-[0032]; App 08/615,012, 7/7/1997 Amendment, pages 2-7.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT J**  
**AU Optronics USP 5,748,266**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
pillars of a color filter	L	<p>pillars associated with and constructed on the color filter, for maintaining separation between the array substrate and the color filter substrate</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 4:65-5:6, and Fig. 8; 5:57-6:5; 6:26-43, 6:47-51, and Figs. 6-11, esp. element 78; 7:4-32, and Fig. 8; 8:20-23; claims 1-5, 7, 9, and 10.</p>	<p>patterned structures that protrude toward the pixel array, to act as a spacer, and are made of color filter material</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:13-19; 3:66-4:21; 4:21-30; 4:31-49; 4:51-64; 4:65-5:06; 5:07-10; 5:57-6:05; 7:09-14; 7:32-43; 7:44-60; 7:62-8:39; 8:40-45; Figures 1-11; JP H08-262484 at paragraphs [0017]-[0032]; App 08/615,012, 7/7/1997 Amendment, pages 2-7.</p>
injecting liquid crystal between the array substrate and the color filter substrate	L	<p>Introducing liquid crystal into the space between the array substrate and the color filter substrate</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:17-18, and Fig. 2; 6:26-43, 6:47 51, and Figs. 6-11; 7:51-8:39, esp. 8:35-39; claim 9; U.S. Patent No. 5,181,132 (Shindo et al.) in general, esp.: 2:9-18 and Fig. 2; 2:19-37 and Fig. 3; 10:39-49 and Fig. 10; 11:15-22 and Fig. 12; 13:27-32 and Fig. 16. U.S. Patent No. 5,338,240 (Kim) in general, esp.: 1:64-66 and Fig.1; 4:31-34 and Fig. 3.</p>	<p>providing liquid crystal through an injection hole between the sealed array and color filter substrates</p> <p><u>Intrinsic Support</u></p> <p>7:62-8:39</p>

# **EXHIBIT K**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT K**  
**AU Optronics USP 6,689,629**

<b>Claim Terms</b>	<b>Des.</b>	<b>Agreed Constructions</b>
connection pads	L	conductive patterns on the substrate that electrically connect the plurality of wiring to circuits located external to the substrate

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
a layer of an insulating substrate, having an area	L	<p>plain meaning</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:12-20, esp. 14-20; 1:32-46, esp. 39-44; 2:13-24, esp. 17-21; 3:11-28, esp. 11-14; 3:29-47, esp. 29-37; 4:33-41; 6:17 34, esp. 23-27, 30-34; claims 1, 9; Figures 1, 5a-5c, 11, 12a-12b; May 29, 2003 Office Action, esp. at 2. U.S. Patent No. 5,285,301 (Shirahashi et al.) 3:37-44, esp. 39-40.</p> <p>Included is the intrinsic support for the disputed term: "area".</p>	<p>material deposited and patterned on a substrate, such as glass, that covers part of the array substrate surface</p> <p><u>Intrinsic Support</u></p> <p>1:7-11; 1:21-2:63; 2:67- 3:6; 3:12-22; 3:26-28; 3:30-51; 3:60-4:23; 4:39-42; 4:55-5:26; 5:29-43; 5:46-6:6; 6:9-47; 6:59-67; 7:5-19; 7:24-27; 7:31-40; 7:50-62; Figs. 2-5, 8, 9, 10; App 10/068,500, 5/29/2003, Office Action, page 2-4.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT K**  
**AU Optronics USP 6,689,629**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
area	A	<p>a specified region</p> <p><u>Intrinsic Support</u></p> <p>1:61-67, esp. 63-66; 2:51-62, esp. 51-54; 3:11-28, esp. 18-19; 3:29-47, esp. 38-39; 5:29-42, esp. 29-33, 38-42; 5:43-53; 5:54-60, esp. 54-57; 5:61-6:6, esp. 5:61-6:1, 6:4-6; 6:35-47, esp. 35-40; claims 1, 9; Japanese Laid Open No. H10-90706, esp. at TR 0003, 0015, 0017, 0020, 0023, 0024, and Figure 5; May 29, 2003 Office Action, esp. at 2. U.S. Patent No. 5,285,301 (Shirahashi et al.) 11:11-14; 11:54-58.</p>	<p>Indefinite</p> <p>or</p> <p>(see above)</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT K**  
**AU Optronics USP 6,689,629**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
a plurality of wiring arranged on the insulating substrate	L	<p>two or more conductive paths disposed on the insulating substrate</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:12-20, esp. 14-20; 1:28-30; 1:32-46, esp. 39-44; 2:13-24, esp. 17-21; 3:11-28, esp. 13-24; 3:29-47, esp. 32-47; 4:33-41, esp. 38-41; 5:29-42, esp. 29-33, 38-42; 6:17-34, esp. 23-27, 30-34; 6:35-47, esp. 35-40; claims 1, 2, 10; Figures 1, 3, 4, 5a-5c, 11, 12a-12b; Japanese Laid Open H10-90706, esp. ¶ 0009; Japanese Laid Open H10-240150, esp. ifif 0002, 0003, 0013May 29, 2003 Office Action, esp. at 2. U.S. Patent No. 5,285,301 (Shirahashi et al.) 6:10-20.</p> <p>Included is the intrinsic support for the disputed term: "a layer of an insulating substrate, having an area".</p>	<p>portions of the layer that convey voltages or signals from the connection pads to the thin-film transistors in the pixel array</p> <p><u>Intrinsic Support</u></p> <p>1:8-2:63; 2:66-3:6; 3:14-15; 3:22-29; 3:31-35; 3:42-48; 3:60-4:23; 4:39-42; 4:52-5:28; 5:34-43; 5:55-6:16; 6:24-47; 6:55-7:40; 7:50-62; Abstract; Figs. 2-11; App 10/068,500, 5/29/2003, Office Action, page 2-4.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT K**  
**AU Optronics USP 6,689,629**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
dummy conductive patterns	L A	<p>a metal pattern that does not conduct signals or current used in the operation of the display</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:12-20, esp. 14-20; 1:32-46, esp. 39-44; 1:46-59, esp. 49-54; 2:13-24, esp. 17-21; 3:11-28, esp. 17-22; 3:29-47, esp. 35-41; 3:66-4:2; 5:29-42, esp. 29-33, 38-42; 5:43-53; 6:14-17; 6:37-38; 6:52-55; claims 1, 9; Figures 2-4, 5a-5c. May 29, 2003 Office Action, esp. at 2. U.S. Patent No. 6,163,356 (Song et al.) 7:31-63; 8:27-40; 8:41-67. U.S. Patent No. 5,285,301 (Shirahashi et al.) 6:10-18; 13:30-61, esp. 45-61; claims 3, 4; Figures 1, 14, 15.</p>	<p>portions of the layer that do not receive or convey voltages or signals</p> <p><u>Intrinsic Support</u></p> <p>1:32-67; 2:25-63; 3:3-19; 3:21-29; 3:33-38; 4:34-42; 4:52-55; 5:11-54; 5:64-66; 6:24-38; 6:52-67; 7:15-35; 7:50-63; Abstract; Fig. 2-4.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT K**  
**AU Optronics USP 6,689,629**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes	L	<p>dummy conductive patterns cover at least 30% of the region specified by where the dummy conductive patterns are formed; the dummy conductive patterns are situated between the connection pads and the pixel electrodes</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:12-20, esp. 14-20; 1:32-46, esp. 39-44; 2:13-24, esp. 17-21; 3:11-28, esp. 17-22; 3:29-47, esp. 35-41; 3:66-4:2; 5:29-42, esp. 29-33, 38-42; 5:43-53; 5:54-60, esp. 54-57; 5:61-6:6, esp. 5:61-6:1, 6:4-6; 6:7-17, esp. 9-12, 14-17; 6:17-34, esp. 23-27, 30-34; 6:35-47, esp. 35-40; claims 1, 9; Figures 2-4, 5a-5c. May 29, 2003 Office Action, esp. at 2-3. U.S. Patent No. 6,163,356 (Song et al.) 1:55-64; 7:31-63; 8:27-40; 8:41-67. U.S. Patent No. 5,285,301 (Shirahashi et al.) 6:10-18; 13:30-61, esp. 45-61; claims 3, 4; Figures 1, 14, 15.</p> <p>Included is the intrinsic support for disputed terms: "dummy conductive patterns," "a layer of an insulating substrate, having an area," "area," "pixel electrodes".</p>	<p>approximately 30% or more of the area of the layer is made of dummy conductive patterns that are located between the connection pads and an outer edge of the pixel electrodes in the pixel array</p> <p><u>Intrinsic Support</u></p> <p>1:61-67; 3:3-6; 3:16-20; 3:35-40; 5:30-43; 5:46-6:17; 6:29-48; 7:8-18; 7:50-62; Figs. 2-5, 8, 11; App 10/068,500, 5/29/2003, Office Action.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT K**  
**AU Optronics USP 6,689,629**

Claim Terms	Des.	AUO Construction	LGD Construction
pixel electrode	A	<p>an electrode for applying a driving voltage to a liquid crystal display element in a liquid crystal display</p> <p><u>Intrinsic Support</u></p> <p>1:12-20, esp. 14-20; 4:33-41, esp. 38-41; 4:42-50, esp. 46-48; Figures 1-4; May 29, 2003 Office Action, esp. at 2. U.S. Patent No. 5,285,301 (Shirahashi et al.) 8:36-53, esp. 37-39; 9:48-56; Figure 13. U.S. Patent No. 6,163,356 (Song et al.) 1:61-64.</p>	<p>patterns of transparent electrically conductive material that stores charge to drive the liquid crystal material within an individual element of the liquid crystal display device</p> <p><u>Intrinsic Support</u></p> <p>1:12-21; 4:45-51; 6:48-52; Figs 2-5.</p>
each wiring		<p>each individual wiring in the plurality of wiring</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:12-20, esp. 14-20; 1:32-46, esp. 39-44; 3:11-28, esp. 14-16; 3:29-47, esp. 33-34; 4:33-41, esp. 38-41; claims 1, 9; Figures 1-4, 5a-5c, 11, 12a-12b; Application for Patent, esp. at 14; May 29, 2003 Office Action, esp. at 2-3; August 29, 2003 Amendment, esp. at 3, 5.</p> <p>Included is the intrinsic support for the disputed term: "a plurality of wiring arranged on the insulating substrate".</p>	Indefinite

# **EXHIBIT L**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT L**  
**AU Optronics USP 6,734,944**

<b>Claim Terms</b>	<b>Des.</b>	<b>Agreed Constructions</b>
regulates a cell gap between the first and the second substrates	L	maintains a uniform spacing within a manufacturing tolerance between the two substrates in the display region
a spacer	L A	a pillar formed between the first and second substrates to set or maintain the size of the gap between substrates

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
at least one of the group consisting of	L	at least one of the characteristics listed as (a) through (e)  <u>Intrinsic Support</u>  2:51-54; 6:47-65; claim 4.	Indefinite  or  means one or more of the limitations selected from (a) to (e)  <u>Intrinsic Support</u>  3:55-4:54; 4:56-5:30; 6:47-52; 8:09-20.

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT L**  
**AU Optronics USP 6,734,944**

Claim Terms	Des.	AUO Construction	LGD Construction
elastic coefficient	A	<p>a value that defines the elasticity of the resin, that is, the resin's ability to change shape or volume in response to force, and then return to its original shape or volume.</p> <p><u>Intrinsic Support</u></p> <p>2:58-3:2; 6:15-24; claim 4; January 16, 2002 Office Action, esp. at 5; August 13, 2002 Office Action, esp. at 3; January 28, 2003 Office Action, esp. at 3-5. U.S. Patent No. 6,299,949 (Shioda et al.) in general, esp.: 3:23-36; 13:1-15; 13:59-67.</p>	Indefinite
Dynamic hardness value (DH)		<p>Defined by the formula in the claim</p> <p><u>Intrinsic Support</u></p> <p>3:54-4:17; 7:27-30; claims 1 and 4; May 16, 2002 Response, esp. at 21-22; November 13, 2002 Response, esp. at 22 23; January 28, 2003 Office Action, esp. at 8-9; June 27, 2003 Office Action, esp. at 10-11; November 28, 2003 Response, esp. at 7-8. U.S. Patent No. 6,299,949 (Shioda et al.) in general, esp.: 14:29-15:16.</p>	<p>Indefinite</p> <p><u>Intrinsic Support</u></p> <p>App 09/558,819, 1/16,2002 Office Action, pages 2-3; App 09/558,819, 5/16/2002 Amendment, pages 21-25; App 09/558,819, 8/13/2002 Office Action, pages 2, 5; App 09/558,819, 11/13/2002 Amendment, pages 22-27; App 09/558,819, 1/28/2003 Office Action, pages 2, 8-11; App 09/558,819, 6/27/2003 Office Action, pages 2, 3, 11-13; App 09/558,819, 11/28/2003 Amendment, pages 7-8.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT L**  
**AU Optronics USP 6,734,944**

Claim Terms	Des.	AUO Construction	LGD Construction
Hardness value of plastic deformation (HV)		<p>Defined by the formula in the claim</p> <p><u>Intrinsic Support</u></p> <p>4:18-51; 7:27-30; claims 1 and 4; May 16, 2002 Response, esp. at 21-22; November 13, 2002 Response, esp. at 22 23; January 28, 2003 Office Action, esp. at 8-9; June 27, 2003 Office Action, esp. at 10-11; November 28, 2003 Response, esp. at 7-8. U.S. Patent No. 6,299,949 (Shioda et al.) in general, esp.: 14:29-15:16.</p>	<p>Indefinite</p> <p><u>Intrinsic Support</u></p> <p>App 09/558,819, 1/16/2002 Office Action, pages 2-3; App 09/558,819, 5/16/2002 Amendment, pages 21-25; App 09/558,819, 8/13/2002 Office Action, pages 2, 5; App 09/558,819, 11/13/2002 Amendment, pages 22-27; App 09/558,819, 1/28/2003 Office Action, pages 2, 8-11; App 09/558,819, 6/27/2003 Office Action, pages 2, 3, 11-13; App 09/558,819, 11/28/2003 Amendment, pages 7-8.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT L**  
**AU Optronics USP 6,734,944**

Claim Terms	Des.	AUO Construction	LGD Construction
The length of one side of the upper spacer surface		<p>The length of one side of the upper spacer surface, measured using a tangent line parallel to the substrate, at 90% of the height</p> <p><u>Intrinsic Support</u></p> <p>5:49-6:14, and Figs. 2A and 2B; claims 2 and 4.</p>	<p>Indefinite or</p> <p>The distance between two specific points on opposite sides of the spacer (The location of the two points are determined by where a line that runs parallel to the one side and parallel to the substrate intersects the opposite sides. The location of the parallel line is determined by multiplying the height of the spacer by a constant. The height of the spacer is determined by the shortest perpendicular distance measured from the bottom of the spacer to a line tangent to the top of the spacer and parallel to the substrate)</p> <p><u>Intrinsic Support:</u></p> <p>5:51-6:14; Figures 2A, 2B; JP 2000321580A at paragraphs [0009]-[0041]; App 09/558,819, 1/16,2002 Office Action, pages 2-3; App 09/558,819, 5/16/2002 Amendment, pages 21-25; App 09/558,819, 8/13/2002 Office Action, pages 2, 5; App 09/558,819, 11/13/2002 Amendment, pages 22-27; App 09/558,819, 1/28/2003 Office Action, pages 2, 8-11; App 09/558,819, 6/27/2003 Office Action, pages 2, 3, 11-13.</p>

# **EXHIBIT M**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M**  
**AU Optronics USP 6,778,160**

<b>Claim Terms</b>	<b>Des.</b>	<b>Agreed Constructions</b>
a table for storing	L	logic operable to hold data in table form

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
video signal	L	<p>a signal comprising video information</p> <p><u>Intrinsic Support</u></p> <p>5:6-14, esp. 6-7, 12-14; 6:51-65, esp. 53-60; 7:17-30, esp. 21-25; claims 1, 3, 4, 6; Figure 1; December 12, 2002 Office Action, esp. at 2-3; March 12, 2003 Amendment, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 2-3, 7-8, 10, 12; March 19, 2004 Notice of Allowability, esp. at 2.</p>	<p>a signal carrying a brightness level from a predetermined range</p> <p><u>Intrinsic Support</u></p> <p>4:47-50; 5:07-15; 5:54-65; 6:27-36; 6:51-7:30; 7:31-45; 10:26-40; 10:57-62; Figs. 1, 2, 8.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M**  
**AU Optronics USP 6,778,160**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
a storage for storing the previous brightness level of the video signal input through said input logic	L	<p>memory for storing a previous level of light intensity of a video signal input through input logic</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 3:26-39, esp. 26-30; 5:30-38; claims 8, 12; Figure 1; December 12, 2002 Office Action, esp. at 2-4; March 12, 2003 Amendment, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 3 8, 10-13; March 19, 2004 Notice of Allowability, esp. at 2. U.S. Patent No. 6,333,727 (Mizumaki) Abstract; 3:26-32; 3:39-48; 3:49-55; claims 1, 3, 4.</p> <p>Included is the intrinsic support for disputed terms: "brightness level" and "video signal"</p>	<p>memory that temporarily holds the brightness level of the video signal received from the host through input logic for the previous time increment</p> <p><u>Intrinsic Support</u></p> <p>4:47-50; 5:30-38; 6:11-26; 6:51-7:30; 9:25-39; 9:40-10:14; 10:49-66; Figs. 1, 7; JP 2001-202051A at paragraphs [0010]-[0023].</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M**  
**AU Optronics USP 6,778,160**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
determinator for determining an output brightness level	L	<p>logic, such as a circuitry, for determining an output brightness value</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 3:26-39, esp. 30-34; 4:61-5:6, esp. 4:61-67; 6:37-40; 6:66-7:16, esp. 6:66-7:5; claims 4; Figure 1; December 12, 2002 Office Action, esp. at 2-5; March 12, 2003 Amendment, esp. at 1-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 3:9, 12; March 19, 2004 Notice of Allowability, esp. at 2.</p> <p>Included is the intrinsic support for disputed terms: "brightness level," "the next brightness level of the video signal input to said input logic," "video signal," "so as to make a time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level," "ideal quantity of light in a stationary state," "time integration quantity of a brightness level," "substantially equal"</p>	<p>circuit or logic that determines the output brightness level by applying an offset to the next brightness level that is predetermined based on a difference in quantity of light between the actual and ideal response characteristics of the liquid crystal cell</p> <p><u>Intrinsic Support</u></p> <p>1:51-2:12; 4:42-56; 4:61-67; 5:15-30; 5:30-38; 5:51-65; 6:11-26; 6:37-40; 6:51-7:30; 7:31-45; 8:41-61; 9:01-39; 10:26-40; 10:49-66; Figs. 1, 2, 5A, 5B, 6, 7, 8; JP 2001-202051A at paragraphs [0010]-[0023]; App 09/760,131, 12/22/2003, Appeal Brief, pages 2-13.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M**  
**AU Optronics USP 6,778,160**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
brightness level	A	<p>level of intensity of light</p> <p><u>Intrinsic Support</u></p> <p>2:26-39, esp. 32-37; 2:50-3:2, esp. 2:63-3:2; 3:15-18; 3:35-37; 3:40-59, esp. 56-59; 3:60-4:7, esp. 3:60-64; 4:42-60; 6:4-6; 8:20-34, esp. 30-34; 8:35-40, esp. 38-40; 10:57-67, esp. 57-62; Figures 2, 4-8, 11; December 12, 2002 Office Action, esp. at 2-5; March 12, 2003 Amendment, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 2-8, 10-12; March 19, 2004 Notice of Allowability, esp. at 2. U.S. Patent No. 6,333,727 (Mizumaki) Abstract; 3:26-32; 3:33-38; 3:39-48; 3:49- 55; 3:56-61; 4:7-13; 4:14-22; 4:23-36; 9:7-19, esp. 13-18; claims 1-5. U.S. Patent No. 6,326,938 (Ishida et al.), esp. 1:33-50, esp. 40-42. U.S. Patent No. 5,956,014 (Kuriyama et al.), esp. 1:55-62.</p>	<p>gray scale value or luminance value</p> <p><u>Intrinsic Support</u></p> <p>4:47-50; 5:54-65; 6:51-7:30; 7:31-45; 9:25-39; 9:40-10:14; 10:26-40; 10:57-62; Figures 1, 2, 7, 8.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M**  
**AU Optronics USP 6,778,160**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
the next brightness level of the next video signal input to said input logic	L	<p>plain meaning</p> <p><u>Intrinsic Support</u></p> <p>Summary of the Invention and Detailed Description of the Invention, generally; 6:11-27, esp. 11-17; 6:37-40; 6:66-7:17, esp. 7:13-15; claim 12; Figures 7, 9, 10; December 12, 2002 Office Action, esp. at 2-5; March 12, 2003 Amendment, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 2 8, 10-13; March 19, 2004 Notice of Allowability, esp. at 2. U.S. Patent No. 6,333,727 (Mizumaki) Abstract; 3:26-32; 3:39-48; 3:49-55; 4:14 22; 4:23-36; 7:4-22; 8:23-37; claims 1, 3, 4.</p> <p>Included is the intrinsic support for the disputed term: "video signal"</p>	<p>the brightness level of the video signal received from the host input to the input logic for the next time increment</p> <p><u>Intrinsic Support</u></p> <p>4:47-50; 5:30-38; 6:11-26; 6:51-7:30; 9:25-39; 9:40-10:14; 10:49-66; Figures 1, 7; JP 2001-202051A at paragraphs [0010]-[0023].</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M**  
**AU Optronics USP 6,778,160**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
<p>so as to make a time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level</p>	<p>L</p>	<p>So as to make a time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level; the next brightness level is the brightness level that immediately follows the previous brightness level.</p> <p><u>Intrinsic Support</u></p> <p>8:35-40; 9:8-25, esp. 8-23; claims 4, 5, 12; Figures 2, 4-8, 11; December 12, 2002 Office Action, esp. at 2-5; March 12, 2003 Amendment, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 2 13; March 19, 2004 Notice of Allowability, esp. at 2.</p> <p>Included is the intrinsic support for disputed terms: "time integration quantity of a brightness level," "substantially equal," "ideal quantity of light in a stationary state," "the next brightness level of the next video signal input to said input logic"</p>	<p>so that the quantity of light based on the actual response characteristic of the liquid crystal cell is substantially equal to the quantity of light based on the ideal response characteristic of the liquid crystal cell when the liquid crystal cell is provided with the next brightness level during the next time increment and the previous brightness level before and after the next time increment</p> <p><u>Intrinsic Support</u></p> <p>1:39-43; 1:51-2:12; 4:42-56; 4:61-67; 5:15-30; 5:16-22; 5:66-6:06; 6:11-26; 6:51-7:30; 7:31-45; 8:35-40; 8:41-61; 9:01-39; 10:26-40; 10:49-66; Figures 1, 2, 4, 5A, 5B, 6, 7, 8; JP 2001-202051A at paragraphs [0010]-[0023]; App 09/760,131, 12/22/2003, Appeal Brief, pages 2-13.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M**  
**AU Optronics USP 6,778,160**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
ideal quantity of light in a stationary state	A	<p>the quantity of light emitted by a pixel during one time increment when the pixel is in a non-changing state</p> <p><u>Intrinsic Support</u></p> <p>4:42-60, esp. 42-47; 6:11-27, esp. 14-19; 8:35-40; claims 4, 12; Figures 2, 4-6, 8, 11; December 12, 2002 Office Action, esp. at 2-3; March 12, 2003 Amendment, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 3 4, 7-8, 12; March 19, 2004 Notice of Allowability, esp. at 2.</p>	<p>quantity of light based on the ideal response characteristic of the liquid crystal cell when the liquid crystal cell is provided with the next brightness level during the next time increment and the previous brightness level before and after the next time increment</p> <p><u>Intrinsic Support</u></p> <p>1:39-43; 4:42-56; 5:66-6:06; 7:31-45; 8:35-40; 8:41-61; 9:01-39; 10:26-40; 10:49-66; Figures 2, 4, 5A, 5B, 6, 7, 8; JP 2001-202051A at paragraphs [0010]-[0023].</p>
image displaying liquid crystal cell	L	<p>an image display element with a liquid crystal</p> <p><u>Intrinsic Support</u></p> <p>1:39-45, esp. 39-41; 3:40-59, esp. 40-44; 7:17-30, esp. 25-28; Figure 1; December 12, 2002 Office Action, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 9:12.</p>	<p>an image display element with a liquid crystal that has the ideal response characteristic at the maximum brightness change given the predetermined range of brightness levels</p> <p><u>Intrinsic Support</u></p> <p>2:25-3:02; 5:40-45; 6:51-7:30; 7:31-45; 7:66-8:25; 10:26-40; Figures 1, 2, 3, 7, 8.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M**  
**AU Optronics USP 6,778,160**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
first brightness information for an input pixel	L	<p>a level of light intensity for an input pixel</p> <p><u>Intrinsic Support</u></p> <p>Summary of the Invention and Detailed Description of the Invention, generally; Abstract; 3:27-39, esp. 27-29; 4:61-5:6, esp. 4:61-64; 6:66-7:16, esp. 7:13-15; claims 1, 13; Figures 7, 9, 10; December 12, 2002 Office Action, esp. at 2:4; March 12, 2003, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 3-9, 12, 13; March 19, 2004 Notice of Allowability, esp. at 2. U.S. Patent No. 6,333,727 (Mizumaki) Abstract; 3:26-32; 3:39-48; 3:49-55; 4:14-22; 4:23-36; 7:4-22; 8:23-37; claims 1, 3, 4.</p> <p>Included is the intrinsic support for disputed terms: "pixel" and "brightness level".</p>	<p>the brightness level of an input signal for a pixel</p> <p><u>Intrinsic Support</u></p> <p>4:47-50; 5:07-15; 5:30-38; 5:54-65; 6:11-26; 6:27-36; 6:51-7:30; 7:31-45; 9:25-39; 9:40-10:14; 10:26-40; 10:49-66; Figures 1, 2, 7, 8; JP 2001-202051A at paragraphs [0010]-[0023].</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M**  
**AU Optronics USP 6,778,160**

Claim Terms	Des.	AUO Construction	LGD Construction
pixel	L	<p>abbreviation for "picture element"</p> <p><u>Intrinsic Support</u></p> <p>1:39-45, esp. 43-45; 2:44-49, esp. 44-47; 2:50-3:2, esp. 50-54; 3:40-59, esp. 40-50; 3:60-4:7, esp. 3:64-4:4; 4:42-60, esp. 42-47; 5:51-65, esp. 54-65; 5:67-6:3, claims 4, 7, 9, 10; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 2:7, 10-12. U.S. Patent No. 6,333,727 (Mizumaki) Abstract; 2:23-33, esp. 23-27; 3:26-32; 3:39-48; 3:49-55; 4:14-22; 4:23-36; 7:4-22; 7:46-60, esp. 56-60; 8:23-37, esp. 23-25; claims 1, 3, 4; Figure 6. U.S. Patent No. 5,483,634 (Hasegawa) 4:23-57, esp. 30-36. U.S. Patent No. 6,064,359 (Lin et al.) 1:12 18, esp. 12-15; 1:21-34, esp. 28-31; 1:35-58, esp. 46-49; 4:60-5:4, esp. 1-4.</p>	<p>an image display element with a liquid crystal that has the ideal response characteristic at the maximum brightness change</p> <p><u>Intrinsic Support</u></p> <p>2:25-3:02; 5:40-45; 6:51-7:30; 7:31-45; 7:66-8:25; 10:26-40; Figures 1, 2, 3, 7, 8.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M**  
**AU Optronics USP 6,778,160**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
frame buffer	L	<p>storage for video information contained in a frame</p> <p><u>Intrinsic Support</u></p> <p>5:30-38, esp. 30-36; 6:11-27; 6:66-7:16, esp. 7:5-10; claims 8, 12, 13; Figure 1; December 12, 2002 Office Action, esp. at 2 5; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 3-8,10-13; March 19, 2004 Notice of Allowability, esp. at 2. U.S. Patent No. 5,347,294 (Usui et al.) 4:64-67, esp. 64-65; 9:28-32, esp. 28-31; 12:53-57, esp. 53-55, U.S. Patent No. 6,333,727 (Mizumaki) 3:26-32; 5:10-18, esp. 15-18; 6:8-11. U.S. Patent No. 5,483,634 (Hasegawa) 4:26-28, esp. 26-27.</p>	<p>a memory circuit or device that temporarily holds brightness levels for all pixels that form one complete picture on the liquid crystal display</p> <p><u>Intrinsic Support</u></p> <p>1:43-45; 5:31-33; 6:11-26; 6:51-7:30; 9:25-39; 9:40-10:14; 10:49-66; Figures 1, 7.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M**  
**AU Optronics USP 6,778,160**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
second brightness information for the next input pixel	L	<p>a level of light intensity for a next input pixel</p> <p><u>Intrinsic Support</u></p> <p>Summary of the Invention and Detailed Description of the Invention, generally; Abstract; 3:26-39, esp. 30-37; 4:61-5:6, esp. 4:61-67; 6:66-7:16, esp. 7:13-15; claims 2, 12; Figures 7, 9, 10; December 12, 2002 Office Action, esp. at 2-4; March 12, 2003, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 3-9, 12, 13; March 19, 2004 Notice of Allowability, esp. at 2. U.S. Patent No. 6,333,727 (Mizumaki) Abstract; 3:26-32; 3:39-48; 3:49-55; 4:14-22; 4:23-36; 7:4-22; 8:23-37; claims 1, 3, 4.</p> <p>Included is the intrinsic support for disputed terms: "pixel" and "brightness level".</p>	<p>the brightness level for the next frame of the input signal for the pixel</p> <p><u>Intrinsic Support</u></p> <p>4:47-50; 5:30-38; 6:11-26; 6:51-7:30; 9:25-39; 9:40-10:14; 10:49-66; Figures 1, 7; JP 2001-202051A at paragraphs [0010]-[0023].</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M**  
**AU Optronics USP 6,778,160**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
an offset for making the time integration quantity of a brightness change substantially equal to an ideal light quantity which is the brightness in a stationary state to said second brightness information	L	<p>a modification of the second brightness information for making the time integration quantity of the brightness change substantially equal to an ideal light quantity which is the brightness in a stationary state</p> <p><u>Intrinsic Support</u></p> <p>2:4-12, esp. 4-10; 5:15-21; 5:22-29, esp. 27-29; 9:1-7; 9:8-24, esp. 8-23; 9:40-63; claims 4, 5; Figures 2, 7-8; December 12, 2002 Office Action, esp. at 2-5; March 12, 2003, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 2-13; March 19, 2004 Notice of Allowability, esp. at 2.</p> <p>Included is the intrinsic support for disputed terms: "time integration quantity of a brightness level," "substantially equal," "ideal light quantity which is the brightness in a stationary state," "brightness level".</p>	<p>a value predetermined based on difference in quantity of light between the actual and ideal response characteristics of the pixel so that the quantity of light based on the actual response characteristic of the pixel to be substantially equal to the quantity of light based on the ideal response characteristic of the pixel when the pixel is provided with the second brightness level during the next frame and the first brightness level before and after the next frame</p> <p><u>Intrinsic Support</u></p> <p>1:39-43; 1:51-2:12; 4:42-56; 4:61-67; 5:15-30; 5:30-38; 5:51-65; 5:66-6:06; 6:11-26; 6:37-40; 6:51-7:30; 7:31-45; 8:35-40; 8:41-61; 9:01-39; 10:26-40; 10:49-66; Figures 1, 2, 4, 5A, 5B, 6, 7, 8; JP 2001-202051A at paragraphs [0010]-[0023]; App 09/760,131, 12/22/2003, Appeal Brief, pages 2-13.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M**  
**AU Optronics USP 6,778,160**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
time integration quantity of a brightness change	A	<p>a quantity of light equal to the actual brightness level output through a liquid crystal, summed over a time period including the rise and fall response time of the liquid crystal</p> <p><u>Intrinsic Support</u></p> <p>4:42-60, esp. 53-56; 8:20-34, esp. 30-34; 11:1-9, esp. 1-4; claims 5, 11; Figures 4-6, 11; December 12, 2002 Office Action, esp. at 2:5; March 12, 2003, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 3-9, 12; March 19, 2004 Notice of Allowability, esp. at 2.</p> <p>Included is the intrinsic support for the disputed term: "brightness level".</p>	<p>Indefinite</p> <p>or</p> <p>quantity of light based on the actual response characteristic of the liquid crystal cell when the liquid crystal cell is provided with the next brightness level during the next time increment and the previous brightness level before and after the next time increment</p> <p><u>Intrinsic Support</u></p> <p>1:39-43; 4:42-56; 4:61-5:06; 5:16-22; 5:66-6:06; 7:31-45; 8:41-61; 9:01-39; 10:26-40; 10:49-66; Figures 2, 5A, 5B, 6, 7, 8; JP 2001-202051A at paragraphs [0010]-[0023].</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M**  
**AU Optronics USP 6,778,160**

Claim Terms	Des.	AUO Construction	LGD Construction
ideal light quantity which is the brightness in a stationary state	A	<p>the quantity of light emitted by a pixel during one time increment when the pixel is in a non-changing state</p> <p><u>Intrinsic Support</u></p> <p>4:42-60, esp. 42-47; 6:11-27, esp. 11-19; 8:35-40; 10:49-56, esp. 49-52; claims 4, 12; Figures 2, 4-6, 8, 11; December 12, 2002 Office Action, esp. at 2:3; March 12, 2003, esp. at 2-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 3-4, 7-8, 12; March 19, 2004 Notice of Allowability, esp. at 2.</p> <p>Included is the intrinsic support for the disputed term: "brightness level".</p>	(see above term)

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT M**  
**AU Optronics USP 6,778,160**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
substantially equal		<p>a level that is not completely the same but can be accepted as a substantially equal level</p> <p><u>Intrinsic Support</u></p> <p>4:42-60, esp. 56-58; 8:41-61, esp. 45-47; 9:26-39, esp. 32-35; claim 4; Figures 4-6, 11; December 12, 2002 Office Action, esp. at 2-3; March 12, 2003, esp. at 1-3; May 19, 2003 Office Action, esp. at 2-6; December 22, 2003 Appeal Brief, esp. at 2-10, 12; March 19, 2004 Notice of Allowability, esp. at 2. U.S. Patent No. 6,333,727 (Mizumaki) Abstract; 3:33-38; 3:56-61; 4:7-13; 4:23-36; 7:4-22; 8:38-57; 9:7-19; claims 1-5.</p>	<p>Indefinite or</p> <p>A level which is not completely the same but can be accepted as a substantially equivalent level, and includes a level which is closer to an ideal quantity of light than no preventive measures are taken.</p> <p><u>Intrinsic Support</u></p> <p>4:56-60.</p>

# **EXHIBIT N**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT N**  
**AU Optronics USP 6,976,781**

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
on outer surfaces of said first edge a plurality of first hooks are formed to protrude outwardly	L	<p>an outer surfaces of said first edge a plurality of first protruding structures, intended to be inserted into a hole for the purpose of fastening one element to another, are formed to protrude outwardly</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term "hooks"</p>	<p>two or more protrusions that are part of the frame and that extend outwardly from the first edge for fastening the frame to the bezel</p> <p><u>Intrinsic Support</u></p> <p>1:44-2:25; 2:28-32; 3:4-21, 31-42, 49-66; 4:16-22, 26-33; Figs. 1, 2, 3, 4 and 5; App 10/446,103, 9/28/2004 Office Action, pages 4-8; App 10/446,103, 1/28/2005 Response, pages 5, 6, 8-10; 13-14; App 10/446,103, 3/8/2005 Final Office Action, pages 3-5, 7-9; App 10/446,103, 6/8/2005 Response, page 5; App 10/446,103, 6/27/2005 Notice of Allowability, pages 2-3.</p>
hooks	A	<p>Any protruding structure intended to be inserted into a hole for the purpose of fastening one element to another</p> <p><u>Intrinsic Support</u></p> <p>1:44-53; 1:54-63; 3:4-13; 3:14-21; Figures 1-5, including those portions of the specification discussing the same; U.S. Patent No.: 5,570,267 (Ma): 2:3-45, esp. 2:41-42, and Figure 2, element 32.</p>	(see above term)

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT N**  
**AU Optronics USP 6,976,781**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
on outer surfaces of said second sidewall a plurality of second hooks are formed to protrude outwardly	L	<p>on outer surfaces of said second sidewall a plurality of second protruding structures, intended to be inserted into a hole for the purpose of fastening one element to another, are formed to protrude outwardly</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term "hooks."</p>	<p>two or more protrusions that are part of the bezel and that extend outwardly from the second sidewall for fastening the bezel to the frame</p> <p><u>Intrinsic Support</u></p> <p>1:44-2:25, 28-32; 3:4-21, 31-42, 49-66; 4:16-22, 26-33; Figs. 1, 2, 3, 4 and 5; App 10/446,103, 9/28/2004 Office Action, pages 4-8; App 10/446,103, 1/28/2005 Response, pages 5, 6, 8-10; 13-14; App 10/446,103, 3/8/2005 Final Office Action, pages 3-5, 7-9; App 10/446,103, 6/8/2005 Response, page 5; App 10/446,103, 6/27/2005 Notice of Allowability, pages 2-3.</p>
as said frame is mounted onto said bezel	L	<p>during the process of mounting the frame onto the bezel</p> <p><u>Intrinsic Support</u></p> <p>3:22-42, esp. 3:34-42; January 28, 2005 Amendment, esp. at 8, amendment to Claim 1 ("Listing of Current Claims")</p>	<p>at the same time when the frame and bezel are joined</p> <p><u>Intrinsic Support</u></p> <p>1:44-2:25; 2:28-32; 3:4-21, 31-42, 49-66; 4:16-22, 26-33; Figs. 1, 2, 3, 4 and 5; App 10/446,103, 9/28/2004 Office Action, pages 4-8; App 10/446,103, 1/28/2005 Response, pages 5, 6, 8-10; 13-14; App 10/446,103, 3/8/2005 Final Office Action, pages 3-5, 7-9; App 10/446,103, 6/8/2005 Response, page 5; App 10/446,103, 6/27/2005 Notice of Allowability, pages 2-3.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT N**  
**AU Optronics USP 6,976,781**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
bezel	A	<p>A frame, typically made of metal</p> <p><u>Intrinsic Support</u></p> <p>1:30-43, esp. 1:33 and Figure 1, element 110; 2:33-50, esp. 2:38-39; 3:14-21, esp. 3:14-18 and Figure 4; 4:7-22, esp. 4:7-9; U.S. Patent No.: 6,170,956 (Rumsey et al.): 5:58-65, esp. 5:61 and Figure 2, element 12; 10:34-11:10, esp. 11:6 and Figure 17, element 117; 12:15-44, esp. 12:15-17 and Figures 17 and 18, element 117; U.S. Patent No.: 6,386,722 (Okumura): 1:20-34, esp. 1:26-27; 3:53-65, esp. 3:53-55, 3:59-60, and Figure 1, element 40.</p>	<p>the outermost back cover for the backlight module</p> <p><u>Intrinsic Support</u></p> <p>1:30-43; 1:66-2:7; 3:14-31; 4:7-9; Figs. 1, 2, 3, 4 and 5.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT N**  
**AU Optronics USP 6,976,781**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
on outside surfaces of said first edge first hooks are formed to protrude outwardly	L	<p>on outside surfaces of said first edge first protruding structures, intended to be inserted into a hole for the purpose of fastening one element to another, are formed to protrude outwardly</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term "hooks."</p>	<p>two or more protrusions that are part of the frame and that extend outwardly from the first edge for fastening the frame to the bezel</p> <p><u>Intrinsic Support</u></p> <p>1:44-2:25; 2:28-32; 3:4-21, 31-42, 49-66; 4:16-22, 26-33; Figs. 1, 2, 3, 4 and 5; App 10/446,103, 9/28/2004 Office Action, pages 4-8; App 10/446,103, 1/28/2005 Response, pages 5, 6, 8-10; 13-14; App 10/446,103, 3/8/2005 Final Office Action, pages 3-5, 7-9; App 10/446,103, 6/8/2005 Response, page 5; App 10/446,103, 6/27/2005 Notice of Allowability, pages 2-3.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT N**  
**AU Optronics USP 6,976,781**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
on outside surfaces of said fourth edge second hooks are formed to protrude outwardly	L	<p>on outside surfaces of said fourth edge second protruding structures, intended to be inserted into a hole for the purpose of fastening one element to another, are formed to protrude outwardly</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term "hooks."</p>	<p>two or more protrusions that are part of the frame and that extend outwardly from the fourth edge for fastening the frame to the bezel</p> <p><u>Intrinsic Support</u></p> <p>1:44-2:25; 2:28-32; 3:4-21, 31-42, 49-66; 4:16-22, 26-33; Figs. 1, 2, 3, 4 and 5; App 10/446,103, 9/28/2004 Office Action, pages 4-8; App 10/446,103, 1/28/2005 Response, pages 5, 6, 8-10; 13-14; App 10/446,103, 3/8/2005 Final Office Action, pages 3-5, 7-9; App 10/446,103, 6/8/2005 Response, page 5; App 10/446,103, 6/27/2005 Notice of Allowability, pages 2-3.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT N**  
**AU Optronics USP 6,976,781**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
on outer surfaces of said second sidewall a plurality of first hooks are formed to protrude outwardly	L	<p>on outer surfaces of said second sidewall a plurality of first protruding structures, intended to be inserted into a hole for the purpose of fastening one element to another, are formed to protrude outwardly</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term "hooks."</p>	<p>two or more protrusions that are part of the bezel and that extend outwardly from the second sidewall for fastening the bezel to the frame</p> <p><u>Intrinsic Support</u></p> <p>1:44-2:25; 2:28-32; 3:4-21, 31-42, 49-66; 4:16-22, 26-33; Figs. 1, 2, 3, 4 and 5; App 10/446,103, 9/28/2004 Office Action, pages 4-8; App 10/446,103, 1/28/2005 Response, pages 5, 6, 8-10; 13-14; App 10/446,103, 3/8/2005 Final Office Action, pages 3-5, 7-9; App 10/446,103, 6/8/2005 Response, page 5; App 10/446,103, 6/27/2005 Notice of Allowability, pages 2-3.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT N**  
**AU Optronics USP 6,976,781**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
on outer surfaces of said first edge a plurality of second hooks are formed to protrude outwardly	L	<p>on outer surfaces of said first edge a plurality of second protruding structures, intended to be inserted into a hole for the purpose of fastening one element to another, are formed to protrude outwardly</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term "hooks."</p>	<p>two or more protrusions that are part of the frame and that extend outwardly from the first edge for fastening the frame to the bezel</p> <p><u>Intrinsic Support</u></p> <p>1:44-2:25; 2:28-32; 3:4-21, 31-42, 49-66; 4:16-22, 26-33; Figs. 1, 2, 3, 4 and 5; App 10/446,103, 9/28/2004 Office Action, pages 4-8; App 10/446,103, 1/28/2005 Response, pages 5, 6, 8-10; 13-14; App 10/446,103, 3/8/2005 Final Office Action, pages 3-5, 7-9; App 10/446,103, 6/8/2005 Response, page 5; App 10/446,103, 6/27/2005 Notice of Allowability, pages 2-3.</p>
simultaneously said second edge is disposed onto outside surfaces of said second sidewall, and said first hooks are inserted and engaged in said second holes for fastening said frame and said bezel	L	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>3:22-42, esp. 3:34-42; January 28, 2005 Amendment, esp. at 8 , amendment to Claim 1 ("Listing of Current Claims")</p>	<p>the first hooks are inserted and engaged with the second holes at the same time the second hooks are inserted and engaged with the first holes to join the frame and bezel</p> <p><u>Intrinsic Support</u></p> <p>1:44-2:25; 2:28-32; 3:4-21, 31-42, 49-66; 4:16-22, 26-33; Figs. 1, 2, 3, 4 and 5.</p>

# **EXHIBIT O**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT O**  
**AU Optronics USP 7,090,506**

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
a first flexible printed circuit board, electrically connecting the display module and the system	L	<p>a first printed circuit made on a flexible film that electrically connects the display module and the system</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:12-21, and Fig. 1; 1:25-34; 1:60-2:5, esp. 1:65-67, and Fig. 2; 2:38-48, and Figs 4a and 4b; claims 1, 5, 9, 13, 17 and 20; October 28, 2005 Office Action, esp. at 2-3; February 14, 2006 Office Action, esp. at 2; May 10, 2006 Response, esp. at 10. U.S. Patent Application Publication No. 2005/0185127 A1 (Fujiyama et al.) in general, esp. 0026 and Figs. 1, 5.</p>	<p>a first flexible film with conductive patterns printed on its surface that electrically connects the display module and the system</p> <p><u>Intrinsic Support</u></p> <p>1:25-35; 1:60-2:25, 40-9, 58-66; Figs. 2, 3a, 3b; 4a, 4b; App 10/921,462, 2/14/06 Office Action, pages 2-3; App 10/921,462, 5/10/06 Response, pages 9-14.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT O**  
**AU Optronics USP 7,090,506**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
display module	A	<p>an LCD module</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:7-10; 1:11-21, and Fig. 1; 1:25-34; 1:60-2:15, and Fig. 2; 2:61-64; 3:2-6; 3:7-15; claims 1, 5-9, 13-17, and 20-23; October 28, 2005 Office Action, esp. at 2-3; February 14, 2006 Office Action, esp. at 2; May 10, 2006 Response, esp. at 10. U.S. Patent Application Publication No. 2005/0185127 A1 (Fujiyama et al.) in general, esp.: Abstract; 0003; 0008; 0018 and Fig. 1. U.S. Patent No. 5,684,550 (Shibata et al.) in general, esp.: Abstract; 3:63-67 and Figs. 23, 24(a)-24(E); 17:16-47 and Figs. 23-39.</p>	<p>an assembly that includes an LCD panel, a touch panel and a light source</p> <p><u>Intrinsic Support</u></p> <p>1:13-21, 25-35, 61-65; 2:58-64; 3:2-6; Figs. 1 and 2.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT O**  
**AU Optronics USP 7,090,506**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
a second flexible printed circuit board, electrically connecting the display module and the first flexible printed circuit board	L	<p>a second printed circuit made on a flexible film that electrically connects the display module and the first printed circuit made on a flexible film</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:12-21, and Fig. 1; 1:25-34; 1:60-2:15, esp. 2:6-15, and Fig. 2; 2:38-57, and Figs 4a and 4b; claims 1, 6, 7, 9, 14, 15, 17, 21, and 22; October 28, 2005 Office Action, esp. at 2-3; February 14, 2006 Office Action, esp. at 2; May 10, 2006 Response, esp. at 10.</p> <p>U.S. Patent Application Publication No. 2005/0185127 A1 (Fujiyama et al.) in general, esp. 0026 and Figs. 1, 5.</p>	<p>a second flexible film with conductive patterns printed on its surface that electrically connects the display module and the first flexible film</p> <p><u>Intrinsic Support</u></p> <p>1:25-35; 1:60-2:25, 40-9, 58-66; Figs. 2, 3a, 3b; 4a, 4b; App 10/921,462, 2/14/06 Office Action, pages 2-3; App 10/921,462, 5/10/06 Response, pages 9-14.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT O**  
**AU Optronics USP 7,090,506**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
the first and second flexible printed circuit boards are joined by hot bar soldering	L	<p>the first and second printed circuits made on flexible film are joined by a soldering process where the solder and flux are applied to the contact area and the contact area is heated with a bar to melt the solder</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:25-34, esp. 1:30-34; 1:60-2:15, and Fig. 2; 2:16-37, and Figs. 2, 3a, and 3b; 2:64-67; claim 1; October 28, 2005 Office Action, esp. at 2-3. U.S. Patent Application Publication No. 2005/0185127 A1 (Fujiyama et al.) in general, esp.: 0021, 0045, and Fig. 1.</p>	<p>both flexible printed circuit boards are connected to each other by a soldering process where the circuit boards are heated with a bar to melt the solder at multiple points simultaneously along each circuit board while pressure is applied to the connection</p> <p><u>Intrinsic Support</u></p> <p>1:25-35; 2:6-37, 46-49, 58-67; Figs. 2, 3a, 3b; App 10/921,462, 2/14/06 Office Action, pages 2-3; App 10/921,462, 5/10/06 Response, pages 9-14; .App 10/921,462, 5/19/06 Notice of Allowability, page 2.</p>
the first and second flexible printed circuit boards are joined by anisotropic conductive film (ACF) bonding	L	<p>both flexible circuit boards are connected to each other by a material that is conductive in one direction after being pressed between the two circuit boards</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:25-34, esp. 1:30-34; 2:40-57, and Figs. 2, 4a, and 4b; 2:64-67; claim 9; October 28, 2005 Office Action, esp. at 2-3. U.S. Patent Application Publication No. 2005/0185127 A1 (Fujiyama et al.) in general, esp.: 0042, 0055, and Figs. 1, 5.</p>	<p>both flexible printed circuit boards are connected to each other by a process where a material that is conductive in one direction is pressed between the two circuit boards</p> <p><u>Intrinsic Support</u></p> <p>1:25-35; 2:6-20, 40-49, 58-67; Figs. 2, 4a, 4b; App 10/921,462, 2/14/06 Office Action, pages 2-3; App 10/921,462, 5/10/06 Response, pages 9-14; .App 10/921,462, 5/19/06 Notice of Allowability, page 2.</p>

# **EXHIBIT P**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT P**  
**AU Optronics USP 7,101,069**

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
a fitting portion	L	<p>a structure for accommodating an illumination tube</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:43-52, esp. 44-45; 1:57-65, esp. 62-65; 2:39-43; 2:50-54; 2:55-3:2, esp. 2:63-3:2; 3:9-14, esp. 9-10; claims 1, 3, 7, 8, 16-18; Figures 3, 4, 5A-5G; May 3, 2005 Office Action, esp. at 2-3; January 9, 2006 Response After Final Rejection, esp. at 6.</p>	<p>the portion of the support designed to hold an illumination tube</p> <p><u>Intrinsic Support</u></p> <p>1:64-65; 2:41-43; 2:50-53; 2:62-3:3; Abstract; Figs. 3, 5A-G; App 10/613,493, 1/9/06 Response, pages 2, 4-7; App 10/613,493, 4/20/06 Notice of Allowability, page 2.</p>
comprises two side walls extending upwardly and separately	L	<p>having at least two sidewalls extending upwardly and separately</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:43-52, esp. 44-45; 1:57-65, esp. 62-65; 2:39-43; 2:50-54; 2:55-3:2, esp. 2:63-64; 3:9-14; claims 1, 7, 8, 16-18; Figures 3, 4, 5A-5G; May 3, 2005 Office Action, esp. at 2; October 20, 2005 Office Action, esp. at 2-3; January 9, 2006 Response After Final Rejection, esp. at 6; April 20, 2006 Notice of Allowability. JP 2001-210126, esp. ¶¶ 0012, 0014, 0016-0020, 0030, 0038 and Figures 4-5.</p>	<p>includes two upright structures that are spaced apart and that are designed to hold the illumination tube</p> <p><u>Intrinsic Support</u></p> <p>2:44-9, 55-61; Figs. 5B, 5C, 5F, and 5G; App 10/613,493, 1/9/06 Response, pages 2, 4-7; App 10/613,493, 4/20/06 Notice of Allowability, page 2.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT P**  
**AU Optronics USP 7,101,069**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
has two side walls extending upwardly and separately	L	<p>having two sidewalls extending upwardly and separately</p> <p><u>Intrinsic Support</u></p> <p>Figures 3, 4, 5A-5G; claims 1, 7, 8, 16-18; January 9, 2006 Response After Final Rejection, esp. at 6; April 20, 2006 Notice of Allowability. JP 2001-210126, esp. ¶¶ 0012, 0014, 0016-0020, 0030, 0038 and Figures 4-5.</p>	<p>has two upright structures that are spaced apart and that are designed to hold the illumination tube</p> <p><u>Intrinsic Support</u></p> <p>2:44-9, 55-61; Figs. 5B, 5C, 5F, and 5G; App 10/613,493, 1/9/06 Response, pages 2, 4-7; App 10/613,493, 4/20/06 Notice of Allowability, page 2.</p>

# **EXHIBIT Q**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT Q**  
**AU Optronics USP 7,125,157**

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
a first supporting portion, disposed on the frame	L	<p>A first supporting portion, disposed on the frame, wherein the term "supporting portion" has the meaning proposed by AUO (i.e. any structure protruding from the frame (including but not limited to a cylinder or a cuboid) intended to support the optical film).</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term "supporting portion."</p>	<p>a first projection from the frame that supports the film when the backlight is in a first position</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 2:1-8; 4:18-24; 4:48-64; 5:17-22; 5:45-6:8; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>
supporting portion	A	<p>Any structure protruding from the frame, (including but not limited to a cylinder or a cuboid) intended to support the optical film</p> <p><u>Intrinsic Support</u></p> <p>2:61-62; 2:66-3:4; 3:5-3:12; 4:17-24, esp. 4:17-21 and Figures 2A and 2B; 6:4-8, esp. 6:4-6 and Figures 3A and 3B; 6:31-42, esp. 6:40-42 and Figure 3C; 7:39-45 and Figures 4A – 4D; claim 10, 22.</p> <p>Included is the intrinsic support for disputed term "constraining portion."</p>	(see above)

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT Q**  
**AU Optronics USP 7,125,157**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
a second supporting portion, further disposed on the frame	L	<p>A second supporting portion, further disposed on the frame, wherein the term "supporting portion" has the meaning proposed by AUO (i.e. any structure protruding from the frame (including but not limited to a cylinder or a cuboid) intended to support the optical film).</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term "supporting portion."</p>	<p>a second projection from the frame that supports the film when the backlight is rotated from the first position</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 4:48-64; 5:36-6:8; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>
a first constraining portion	L	<p>A first constraining portion, wherein the term "constraining portion" has the meaning proposed by AUO (i.e. any formation on or in the optical film (including but not limited to a hole or a groove) intended to restrict the movement range of the film).</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term "constraining portion."</p>	<p>a first passage through the film that has a gap in the gravity acting direction after receiving a supporting portion</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 2:66-3:19; 5:39-6:3; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 1/25/06 Office Action, pages 8-9; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT Q**  
**AU Optronics USP 7,125,157**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
constraining portion	A	<p>Any formation on or in the optical film (including but not limited to a hole or groove) intended to restrict the movement range of the film</p> <p><u>Intrinsic Support</u></p> <p>2:27-30; 2:63-65; 4:7-16, esp. 4:13-15 and Figure 2A; 6:47-49; 7:22-33, esp. 7:28-29 and Figure 3C; claims 2, 11, 17.</p> <p>Included is the intrinsic support for disputed term "supporting portion."</p>	<p>a passage through the film that has a gap in the gravity acting direction after receiving a supporting portion</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 2:66-3:19; 5:45-6:3; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 1/25/06 Office Action, pages 8-9; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>
a second constraining portion	L	<p>A second constraining portion, wherein the term "constraining portion" has the meaning proposed by AUO (i.e. any formation on or in the optical film (including but not limited to a hole or a groove) intended to restrict the movement range of the film).</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term "constraining portion."</p>	<p>a second passage through the film that has a gap in the gravity acting direction after receiving a supporting portion</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 2:66-3:19; 5:36-6:3; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 1/25/06 Office Action, pages 8-9; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT Q**  
**AU Optronics USP 7,125,157**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
disposed in a first position	L	<p>an initial position of a liquid crystal display unit.</p> <p><u>Intrinsic Support</u></p> <p>2:12-26, esp. 2:19-25; 2:52-60; 2:66-3:4; 4:37-42; 4:48-56, esp. Figure 3A; 5:37-54, esp. 5:39-44 and Figure 3A; 6:14-30, esp. 6:22-27 and Figure 3C; 7:22-33, esp. 7:22-23 and Figure 3C; 7:39-45 and Figures. 4A-4D; 7:46-52, esp. 7:49-50 and Fig. 4A; claim 23.</p> <p>Included is the intrinsic support for disputed term "disposed in a second position."</p>	<p>in an orientation where the first projection is located near an upper edge of the frame</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 2:1-8; 2:66-3:19; 5:36-6:3; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 1/25/06 Office Action, pages 8-9; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>
first position	A	<p>See above construction for "disposed in a first position."</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term "disposed in a first position."</p>	(see above)

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT Q**  
**AU Optronics USP 7,125,157**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
the first supporting portion partially contacts an inner wall of the first constraining portion for positioning the film	L	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>Figures 2A-2B, 3A-3C, 4A-4D; 5:17-22; 5:55-6:3; 6:55-61; 7:22-33; 7:46-8:2.</p>	<p>the first projection touches a top portion of the first passage to support the film and has a gap below the first projection</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 2:1-8; 2:66-3:19; 5:17-22; 5:36-6:3; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 1/25/06 Office Action, pages 8-9; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>
does not contact	L	<p>Plain meaning</p>	<p>does not touch</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 2:1-8; 2:66-3:19; 5:36-6:3; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 1/25/06 Office Action, pages 8-9; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT Q**  
**AU Optronics USP 7,125,157**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
disposed in a second position	L	<p>a second position of a liquid crystal display unit where the position is determined by reference to the angle of rotation between the first position and the second position.</p> <p><u>Intrinsic Support</u></p> <p>2:12-26, esp. 2:19-25; 2:52-60; 3:6-11; 4:37-42; 4:48-56, esp. Figure 3B; 5:55-6:3, esp. 5:55-57 and Figure 3B; 7:22-33, esp. 7:22-23, 7:26-27, and Figure 3C; 7:39-45 and Figures. 4A- 4D; 7:53-59, esp. 7:55-57 and Figure 4B; claim 23.</p> <p>Included is the intrinsic support for disputed term "disposed in a first position."</p>	<p>in an orientation rotated from the first position so that the second projection is located near an upper edge of the frame</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 2:1-8; 2:66-3:19; 5:36-6:3; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 1/25/06 Office Action, pages 8-9; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>
second position	A	<p>See above construction for "disposed in a second position."</p> <p><u>Intrinsic Support</u></p> <p>Same as for the term "disposed in a second position."</p>	(see above)

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT Q**  
**AU Optronics USP 7,125,157**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
the second supporting portion partially contacts an inner wall of the second constraining portion for positioning the film	L	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>Figures 2A-2B, 3A-3C, 4A-4D; 5:17-22; 5:55-6:3; 6:55-61; 7:22-33; 7:46-8:2.</p>	<p>the second projection touches a top portion of the second passage to support the film and has a gap below the second projection</p> <p><u>Intrinsic Support</u></p> <p>1:27-51; 2:1-8; 2:66-3:19; 5:17-22; 5:36-6:3; 6:17-22; 7:21-27; Figs. 2A-B, 3A-C, 4A-D; App 10/902,914, 1/25/06 Office Action, pages 8-9; App 10/902,914, 3/20/06 Response, pages 8-9; App 10/902,914, 5/22/06 Notice of Allowability, pages 2-3.</p>
on opposite corners of the film	L	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>2:47-9; 7:34-9; Fig. 3C.</p>	<p>through areas where two edges of the film intersect such that the areas do not share an edge of the film</p>
on adjacent corners of the film	L	<p>Plain meaning</p> <p><u>Intrinsic Support</u></p> <p>2:47-9; 6:15-22; Fig. 3C.</p>	<p>through areas where two edges of the film intersect such that the areas share one edge of the film</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT Q**  
**AU Optronics USP 7,125,157**

<b>Claim Terms</b>	<b>Des.</b>	<b>AUO Construction</b>	<b>LGD Construction</b>
frame comprising a first supporting portion and a second supporting portion	L	See above constructions for "a first supporting portion, disposed on the frame" and "a second supporting portion, further disposed on the frame."  <u>Intrinsic Support</u>  Same as for the term "supporting portion."	(see constructions above)
a third constraining portion and a fourth constraining portion disposed on the frame		Plain meaning	Indefinite
the third constraining portion and the fourth constraining portion pass through the first constraining portion and the second constraining portion, respectively		Plain meaning	Indefinite

# **EXHIBIT R**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT R**  
**CHI MEI USP 5,619,352**

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
a layer of a birefringent material	L	<p>a layer of material that has varying indices of refraction depending on the direction light travels through the material. An index of refraction is the ratio of the speed of light in a medium relative to the speed of light in a vacuum</p> <p><u>Intrinsic Support</u></p> <p>2:53-3:14; 10:27-11:8; 12:23-38; 16:1-17:35; 17:59-20:51; Fig. 14</p>	<p>a thickness of material including positively birefringent molecules that are uniaxial or near uniaxial in character</p> <p><u>Intrinsic Support</u></p> <p>2:53-3:19; 7:08-22; 8:16-53; 9:37-10:47; 10:51-64; 12:45-50; 13:08-20; 14:48-57; 15:63-67; 16:03-10; Figs. 7-14; Abstract; App 08/223,251, 8/23,1995, Amendment, pages 6-9.</p>
optical symmetry axis	L	<p>the extraordinary optic axis in uniaxial materials and the principal optic axis in biaxial materials. A uniaxial material has two axes with the same index of refraction and another axis, the extraordinary axis, that has a different index of refraction. A biaxial material has three axes each with a different index of refraction, and the axis with the highest index of refraction is the principal optic axis</p> <p><u>Intrinsic Support</u></p> <p>2:61-3:17; 10:27-11:8; 12:23-38; 16:1-17:35; 17:59-20:51; Fig. 14</p>	<p>the extraordinary axis of the molecules</p> <p>or</p> <p>Indefinite</p> <p><u>Intrinsic Support</u></p> <p>2:53-3:19; 9:37-10:47; 10:51-64.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT R**  
**CHI MEI USP 5,619,352**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
tilt angle varies along an axis normal to said layer	L	<p>the tilt angle at a bottom surface of the layer is different than the tilt angle at a top surface of the layer relative to an axis normal (perpendicular) to the layer</p> <p><u>Intrinsic Support</u></p> <p>3:50-61; 11:13-17; 12:42-54; 17:59-20:51; Fig. 2; Fig. 12; Application 08/313,476, Response, January 22, 1996</p>	<p>the tilt angle of the compensator varies along an axis normal to the layer of birefringent material and is limited to values between approximately 25 degrees and approximately 65 degrees</p> <p><u>Intrinsic Support</u></p> <p>7:08-22; 10:65-11:21; 12:23-26; 14:04-07; 14:33-44; 16:16-19; Figs. 7-14; Title &amp; Abstract; App 08/223,251, 8/23,1995, Amendment, pages 6-9 ; App 08/690,033, 1/22/1996, Amendment, pages 9-11.</p>
a desired viewing characteristic over a specified field of view		<p>A contrast ratio that exceeds a threshold for a specified range of viewing angles. The contrast ratio is a luminance at a bright state divided by a luminance at a dark state.</p> <p><u>Intrinsic Support</u></p> <p>1:57-2:21; 5:1-8:42; 10:17-25; 10:49-59; 17:59-20:51; Fig. 4; Fig. 5; Fig. 6; Fig. 7; Fig. 8; Fig. 9; Fig. 10</p>	Indefinite

# **EXHIBIT S**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT S**  
**CHI MEI USP 6,008,786**

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
driver means	L	<p>Function (plain meaning): driving the display cell with grey scale data signals</p> <p>Corresponding structure: X-driver 3, Y-driver 5 (Fig. 1) and equivalents</p> <p><u>Intrinsic Support</u></p> <p>1:27-46; 1:47-52; 6:1-9; and exhibits referenced therein, including Fig. 1</p>	<p>Interpreted per 35 USC §112¶6</p> <p>function: driving the display cell with sets of grey scale data signals</p> <p>structure: Fig. 1, element 3</p> <p><u>Intrinsic Support</u></p> <p>1:27-46; 2:46-3:11; 3:64-4:06; Fig. 1.</p>
data control means	L	<p>Function (plain meaning): receiving gray scale data signals and outputting the gray scale data signals to the driver with a predetermined timing</p> <p>Corresponding structure: computing circuit 32, buffer circuit 26, delay circuit 24 (Fig. 5) and equivalents</p> <p><u>Intrinsic Support</u></p> <p>4:31-37; 5:23-30; 3:25-31; 5:58-63; 6:1-9; and exhibits referenced therein, including Fig. 5</p>	<p>Interpreted per 35 USC §112¶6</p> <p>function: receiving gray scale data signals related to the setting of a gray scale for the display cell and outputting said gray scale data signals to said driver with a predetermined timing</p> <p>structure: Fig. 5, all elements; Figs 6-8</p> <p><u>Intrinsic Support</u></p> <p>1:27-46; 1:66-2:27; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 5:11-43; 5:58-63; Figs. 1, 2, 5, 6, 7.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT S**  
**CHI MEI USP 6,008,786**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
computing means	L	<p>Function (plain meaning): changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium</p> <p>Corresponding structure: computing circuit 32 (Fig. 5) and equivalents</p> <p><u>Intrinsic Support</u></p> <p>4:31-37; 5:58-63; 2:1-23; 3:25-31; 4:55-57; 6:1-9; and exhibits referenced therein, including Fig. 5</p>	<p>Interpreted per 35 USC §112 ¶6</p> <p>function: changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium</p> <p>structure: Fig. 5, elements 32, 33, 34; Figs. 6-8</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 4:55-5:10; 5:11-43; 5:58-63; Figs. 5, 6, 7, 8.</p>
changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level	L	<p>see claim 1 "computing means" above</p>	<p>adding or subtracting compensation values to modify the gray scale levels of one or more, but not all, color video signals</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:27-46; 1:66-2:27; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 4:55-5:10; 5:11-43; 5:58-63; Figs. 1, 2, 5, 6, 7, 8; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT S**  
**CHI MEI USP 6,008,786**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
buffer means	L	<p>plain meaning</p> <p>or, if the Court determines construction is necessary,</p> <p>memory where gray scale data signals can be temporarily stored and delayed</p> <p>if interpreted pursuant to 35 U.S.C. §112, ¶6:</p> <p>Function (plain meaning): delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected</p> <p>Corresponding structure: buffer circuit 26, delay circuit 24 (Fig. 5) and equivalents</p> <p><u>Intrinsic Support</u></p> <p>5:23-30; 4:11-21; 6:1-9; and exhibits referenced therein, including Fig. 5</p>	<p>Interpreted per 35 USC §112¶6</p> <p>function: delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected</p> <p>structure: Fig. 5, element 24</p> <p>Indefinite</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:46-3:11; 3:12-32; 3:64-4:06; 5:11-43; 4:07-56; Figs. 5, 6, 7.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT S**  
**CHI MEI USP 6,008,786**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected	L	see claim 1 "buffer means" above	holding or deferring at least one color video signal that is not subjected to a compensation value by the amount of time taken to modify another color video signal  <u>Intrinsic Support</u>  Abstract; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 5:11-43; Figs. 5, 6, 7; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.
adjusting means	L	Function (plain meaning): varying the amount of correction accorded to the gray scale data signals for said at least one color  Corresponding structure: computing circuit 32 (Fig. 5) and equivalents  <u>Intrinsic Support</u>  5:37-43; 4:31-37; 3:25-31; 5:56-63; 6:1-9; and exhibits referenced therein, including Fig. 5	Interpreted per 35 USC §112 ¶6  function: varying the amount of correction accorded to the gray scale data signals for said at least one color  structure: Fig. 5, elements 33, 34; Figs. 6-8  <u>Intrinsic Support</u>  2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 4:55-5:10; 5:11-43; 5:58-63; Figs. 5, 6, 7, 8.

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT S**  
**CHI MEI USP 6,008,786**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
said adjusting means (claim 3)		<p>Function (plain meaning): delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected</p> <p>Corresponding structure: buffer circuit 26, delay circuit 24 (Fig. 5) and equivalents</p> <p><u>Intrinsic Support</u></p> <p>5:23-30; 4:11-21; 6:1-9; and exhibits referenced therein, including Fig. 5</p>	Indefinite
changing the level of gray scale data signals related to at least one of the multicolors supplied to the display cell to create a corrected gray scale data signal with a level different from the inputted gray scale data signal	L	<p>plain meaning</p> <p>or, if the Court determines construction is necessary,</p> <p>changing the level of gray scale data signals related to at least one of the multicolors supplied to the display cell to create a corrected gray scale data signal</p> <p><u>Intrinsic Support</u></p> <p>4:31-37; 5:58-63; 2:1-23; 3:25-31; 4:55-57; 6:1-9; and exhibits referenced therein</p>	<p>adding or subtracting compensation values to modify the gray scale levels of one or more, but not all, input color video signals</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:27-46; 1:66-2:27; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 4:55-5:10; 5:11-43; 5:58-63; Figs. 1, 2, 5, 6, 7, 8; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT S**  
**CHI MEI USP 6,008,786**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
delaying the output for at least one other of the multicolor by the time taken for correction of said at least one color	L	<p>plain meaning</p> <p>or, if the Court determines construction is necessary,</p> <p>delaying the output for at least one other of the multicolors by the time taken for correction of said at least one color</p> <p><u>Intrinsic Support</u></p> <p>5:23-30; 4:11-21; 6:1-9; and exhibits referenced therein</p>	<p>holding or deferring the output of at least one color video signal that is not subject to a compensation value by the amount of time taken to modify another color video signal</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 5:11-43; Figs. 5, 6, 7; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT S**  
**CHI MEI USP 6,008,786**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
simultaneously output the gray scale data of all said multicolors	L	<p>plain meaning</p> <p>or, if the Court determines construction is necessary,</p> <p>outputting the gray scale data of all the multicolors from a buffer at about the same time</p> <p><u>Intrinsic Support</u></p> <p>3:29-31; 4:19-21; 5:23-30; 4:11-18; 6:1-9; and exhibits referenced therein</p>	<p>provides all multicolor gray scale data to the data driver during the same predetermined time interval</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:27-46; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 5:11-43; Figs. 1, 5, 6, 7; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>
display cells		plain meaning	Indefinite

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT S**  
**CHI MEI USP 6,008,786**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
calculation logic . . . for changing the level of the gray scale data signals of said at least one color to a different gray scale level	L	<p>plain meaning</p> <p>or, if the Court determines construction is necessary,</p> <p>structure, including a driver circuit, that changes the gray scale data signal for at least one color relative to the other colors</p> <p><u>Intrinsic Support</u></p> <p>4:31-37; 5:58-63; 2:1-23; 3:25-31; 4:55-57; 6:1-9; and exhibits referenced therein</p>	<p>calculation logic . . . for adding or subtracting compensation values to modify one or more, but not all, color video signals</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:27-46; 1:66-2:27; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 4:55-5:10; 5:11-43; 5:58-63; Figs. 1, 2, 5, 6, 7, 8; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>
driver circuit for any other of the colors without the calculation logic in its driver circuit	L	<p>plain meaning</p> <p>see claim 7 “calculation logic” above.</p>	<p>at least one color video signal path that does not include calculation logic</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 5:11-43; Figs. 5, 6, 7; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT S**  
**CHI MEI USP 6,008,786**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
delaying the gray scale signals for the other of the colors	L	<p>plain meaning</p> <p>see claim 5 “delaying the output for at least one other of the multicolor by the time taken for correction of said at least one color” above</p>	<p>holding or deferring the output of the unmodified color video signals</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 5:11-43; Figs. 5, 6, 7; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>
said data control means (claim 11)		<p>structure that can add or subtract a binary signal representing a change of at least one gray scale level for at least one color</p> <p>see also claim 7, “calculation logic” below</p> <p><u>Intrinsic Support</u></p> <p>3:25-31; 4:31-37; 5:58-63; 2:1-23; 4:55-57; 6:1-9; and exhibits referenced therein, including Fig. 5</p>	Indefinite

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT S**  
**CHI MEI USP 6,008,786**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
changing the gray scale data signals related to one of the multicolors	L	<p>plain meaning</p> <p>or, if the Court determines construction is necessary,</p> <p>changing the gray scale data signals for at least one of the multicolors</p> <p><u>Intrinsic Support</u></p> <p>4:31-37; 5:58-63; 2:1-23; 3:25-31; 4:55-57; 6:1-9; and exhibits referenced therein</p>	<p>adding or subtracting compensation values to modify the gray scale level of one of the color video signals</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:27-46; 1:66-2:27; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 4:55-5:10; 5:11-43; 5:58-63; Figs. 1, 2, 5, 6, 7, 8; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT S**  
**CHI MEI USP 6,008,786**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
delaying the output for any other color of the multicolors with gray scale data signals not subject to a correction by the amount of time taken for correction of the one color	L	<p>plain meaning</p> <p>or, if the Court determines construction is necessary,</p> <p>delaying the output for any uncorrected color of the multicolors by the amount of time taken for correction of the one color</p> <p><u>Intrinsic Support</u></p> <p>5:23-30; 4:11-21; 6:1-9; and exhibits referenced therein</p>	<p>holding or deferring the output of the remaining color video signals that are not subject to compensation values by the amount of time taken to modify the one color video signal</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 5:11-43; Figs. 5, 6, 7; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>
synchronize the timing of the gray scale data signals for all said multicolors	L	<p>plain meaning</p> <p>see also claim 5 “simultaneously output the gray scale data of all said multicolors” above</p>	<p>provides all multicolor gray scale data signals to the data driver during the same predetermined time interval</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:27-46; 2:46-3:11; 3:12-32; 3:64-4:06; 4:07-56; 5:11-43; Figs. 1, 5, 6, 7; JP H09-319334A at paragraphs [0013]-[0026]; App 08/832,640, 3/23/1999 Amendment, pages 4-7; App 08/832,640, 7/19/1999 Office Action, page 2.</p>

# **EXHIBIT T**

**JOINT CLAIM CONSTRUCTION STATEMENT EXHIBIT T**  
**CHI MEI USP 6,013,923**

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
source line	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>conductor that connects the source terminals of pixel transistors and leads to the source amplifiers</p> <p><u>Intrinsic Support</u></p> <p>4:65-66; 5:1-5:6; 7:22-31; 7:66-8:2 and exhibits referenced therein</p>	<p>a pattern of electrically conductive material that conveys data signals to transistors within the TFT array</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:6-11; 1:12-2:17; 2:58-65; 3:6-31, 3:39-43; 3:45-4:31; 4:64-5:15; 5:27-41; 5:48-6:19; 7:1-31; 7:49-8:2; Figs. 1-3, 6-8.</p>
gate line	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>conductor that connects the gate terminals of pixel transistors and leads to the gate driver circuit</p> <p><u>Intrinsic Support</u></p> <p>4:64-65; 4:66-5:1; 7:22-31; 7:66-8:2 and exhibits referenced therein</p>	<p>a pattern of electrically conductive material that conveys gate signals to transistors within the TFT array</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:6-11; 1:12-2:17; 2:58-65; 3:6-31, 3:39-43; 3:45-4:31; 4:64-5:15; 5:27-47; 5:65-6:19; 7:1-31; 7:49-8:2; Figs. 1-3, 6-8.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT EXHIBIT T**  
**CHI MEI USP 6,013,923**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
during formation of said gate lines	L	<p>during the manufacturing stages in which the gate lines are formed and connected</p> <p><u>Intrinsic Support</u></p> <p>7:22-31; 4:64-5:1; 5:27-40; 7:49-55; 5:41-64; 1:55-62; 7:66-8:2 and exhibits referenced therein</p>	<p>at the same time when the electrically conductive material that forms the gate lines is deposited and etched</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:6-11; 1:12-2:17; 2:58-65; 3:6-31, 3:39-43; 3:45-4:31; 4:64-5:15; 5:27-47; 5:65-6:19; 7:1-31; 7:49-8:2; Figs. 3-9; App. No. 09/000,479, 11/3/1997, PCT International Preliminary Examination Report, pages 2-4.</p>
shorting element	L	<p>plain meaning</p> <p><u>Intrinsic Support</u></p> <p>see, e.g., 1:64-2:3 and exhibits referenced therein</p>	<p>a pattern of conductive material for electrically connecting, with low resistance, the gate lines to each other or the source lines to each other</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:55-2:3; 1:7-10; 1:12-20; 1:24-27; 1:44-2:10; 2:19-28; 2:44-51; 2:58-68; 3:6-30; 3:54-62; 4:5-31; 5:38-64; 6:14-35; 6:47-57; 7:1-21; 7:36-40; 7:49-8:2; Figs. 3-9; App. No. 09/000,479, 11/3/1997, PCT International Preliminary Examination Report, pages 2-4.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT EXHIBIT T**  
**CHI MEI USP 6,013,923**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
protection element	L	<p>element protecting from electrostatic discharge (ESD)</p> <p><u>Intrinsic Support</u></p> <p>5:60-6:13; 4:24-26; 2:61-67; 7:66-8:2 and exhibits referenced therein</p>	<p>a circuit component designed to protect against electrostatic discharge and to allow for testing</p> <p><u>Intrinsic Support</u></p> <p>1:5-10; 1:12-20; 1:24-26; 1:31-43; 1:55-3:43; 3:45-50; 3: 54-61; 4:5-22; 4:27-32; 5:33-41; 5:50-6:13; 6:19-57; 7:15-40; 7:49-8:2; Figs. 3-9; App. No. 09/000,479, 11/3/1997, PCT International Preliminary Examination Report, pages 2-4.</p>
during formation of said source lines	L	<p>during the manufacturing stages in which the source lines are formed and connected</p> <p><u>Intrinsic Support</u></p> <p>7:22-31; 5:1-5:6; 7:49-55; 5:30-34; 5:48-57; 1:55-62; 7:66-8:2 and exhibits referenced therein</p>	<p>at the same time when the electrically conductive material that forms the source lines is deposited and etched</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:6-11; 1:12-2:17; 2:58-65; 3:6-31, 3:39-43; 3:45-4:31; 4:64-5:15; 5:27-41; 5:48-6:19; 7:1-31; 7:49-8:2; Figs. 3-9; App. No. 09/000,479, 11/3/1997, PCT International Preliminary Examination Report, pages 2-4.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT EXHIBIT T**  
**CHI MEI USP 6,013,923**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
electrically coupling said shorting elements	L	<p>electrically connecting the shorting elements</p> <p><u>Intrinsic Support</u></p> <p>5:57-64; 7:66-8:2 and exhibits referenced therein</p>	<p>electrically connecting the shorting elements without intervening protection elements</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:55-2:3; 1:7-10; 1:12-20; 1:24-27; 1:44-2:10; 2:19-28; 2:44-51; 2:58-68; 3:6-30; 3:54-62; 4:5-31; 5:7- 14; 5:38-64; 6:14-35; 6:47-57; 7:1-21; 7:36-40; 7:49-8:2; Figs. 3-9; App. No. 09/000,479, 11/3/1997, PCT International Preliminary Examination Report, pages 2-4.</p>

# **EXHIBIT U**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT U**  
**CHI MEI USP 6,134,092**

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
peripheral portion	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>a portion of the waveguide that is covered by a cover</p> <p><u>Intrinsic Support</u></p> <p>5:9-14; 6:66-7:2; 7:12-15; 9:30-12:9; Fig. 12; Fig. 13</p>	<p>boundary adjacent a side edge</p> <p><u>Intrinsic Support</u></p> <p>1:43-52, 66-67; 3:18-22; 5:9-15; 7:3-15; 7:26-30; 7:55-59; Figs. 5, 6A, 13, 13A.</p>
a series of point light sources	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>three or more solid state light sources</p> <p><u>Intrinsic Support</u></p> <p>1:24-34; 1:54-56; 3:18-22; 7:3-5; 9:30-12:9</p>	<p>a sequence of separate components, such as light-emitting diodes, that provide the desired light that illuminates the waveguide or optical cavity</p> <p><u>Intrinsic Support</u></p> <p>1:61-5; 2:5-9; 3:15-30; 6:45-50; 7:27-31; Figs. 2, 11, 13, and 13A; App 09/057,199, 3/23/00 Notice of Allowability, pages 2-4.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT U**  
**CHI MEI USP 6,134,092**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
diffusive reflective surfaces	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>surfaces, including a surface that extends upward relative to a planar surface, that diffusively reflect light</p> <p><u>Intrinsic Support</u></p> <p>3:44-47; 4:24-54; 5:61-6:7; 7:16-26; 7:44-61; 9:30-12:9; Fig. 2; Fig. 4; Fig. 8; Fig. 13; Fig. 13A</p>	<p>non-transparent boundaries of an object that reflect and scatter light from the point light source</p> <p><u>Intrinsic Support</u></p> <p>1:44-52; 2:10-6; 3:42-4:3; 4:24-54; 6:1-7; 6:44-61; 7:3-15; Figs. 3, 11, 13, 13A; App 09/057,199, 3/23/00 Notice of Allowability, pages 2-4.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT U**  
**CHI MEI USP 6,134,092**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
oriented relative to the series of point light sources and the waveguide so as to introduce light	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>construe:</p> <p>“the diffusive reflective surfaces oriented relative to the series of point light sources and the waveguide so as to introduce light in regions of said waveguide between pairs of said point light sources”</p> <p>to mean:</p> <p>the diffusive reflective surfaces are angled relative to each other to direct light from the point light sources into the waveguide</p> <p><u>Intrinsic Support</u></p> <p>3:54-57; 3:65-4:3; 7:16-23; 7:44-61; 9:30-12:9; Fig. 2; Fig. 3; Fig. 13; Fig. 13A</p>	<p>arranged to be substantially perpendicular to the top surface of the waveguide so as to introduce scattered light reflected directly from the point light sources into the waveguide</p> <p><u>Intrinsic Support</u></p> <p>1:43-52; 3:15-22, 42-4:3; 5:9-15; 7:3-31, 55-9; Figs. 11, 13, 13A.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT U**  
**CHI MEI USP 6,134,092**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
whereby the peripheral portion of the waveguide is substantially uniformly illuminated	L C	<p>not a claim limitation</p> <p>or</p> <p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>The portion of the waveguide, that is covered by a cover and intersects an aperture, is substantially uniformly illuminated. The aperture is an area of the waveguide through which light escapes the illumination device.</p> <p><u>Intrinsic Support</u></p> <p>1:17-23; 5:49-54; 5:9-14; 6:66-7:2; 7:12-15; 7:36-39; 9:30-12:9; Fig. 12; Fig. 13</p>	<p>such that the same or nearly the same amount of light is provided along a boundary adjacent a side edge of the waveguide</p> <p><u>Intrinsic Support</u></p> <p>1:47-52; 2:11-17; 3:15-20, 5:1-8; 7:3-15; 7:55-59.</p>
light-emitting diodes mounted on an electrical-conductive strip of material	L	<p>plain meaning</p>	<p>components, each containing a semiconductor diode chip as part of their structure, that provide the desired light that illuminates the waveguide or optical cavity and that are attached to a strip of material that provides electrical signals to the components</p> <p><u>Intrinsic Support</u></p> <p>3:15-31; 6:45-54; Figs. 2, 13, and 13A.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT U**  
**CHI MEI USP 6,134,092**

Claim Terms	Des.	CMO Construction	LGD Construction
mouth	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>construe:</p> <p>“entry mouth”</p> <p>to mean:</p> <p>a region of the optical cavity that is located nearest to the point light source</p> <p>and construe:</p> <p>“exit mouth”</p> <p>to mean:</p> <p>a region of the optical cavity that is located the farthest from the point light source</p> <p><u>Intrinsic Support</u></p> <p>4:10-23; 7:16-30; 9:30-12:9; Fig. 3; Fig. 13</p>	<p>an optical opening through which light passes</p> <p><u>Intrinsic Support</u></p> <p>4:10-23; 6:48-9; Figs. 2, 3, 10, 13 and 13A.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT U**  
**CHI MEI USP 6,134,092**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
diffusive reflective optical cavities	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>a space between diffusive reflective surfaces</p> <p><u>Intrinsic Support</u></p> <p>3:44-47; 4:24-54; 5:61-6:7; 7:5-12; 7:16-26; 7:44-61; 9:30-12:9; Fig. 2; Fig. 8; Fig. 11; Fig. 12; Fig. 13; Fig. 13A</p>	<p>optical passages having non-transparent surfaces that reflect and scatter light from the point light source</p> <p><u>Intrinsic Support</u></p> <p>1:61-65; 2:1-9; 4:10-23; 7:3-15; 7:44-61; Fig. 13A.</p>
guide members positioned along a periphery of the optical cavity	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>guide members are spaced apart along a side of the optical cavity</p> <p><u>Intrinsic Support</u></p> <p>3:42-44; 9:30-12:9; Fig. 2; Fig. 3; Fig. 11; Fig. 13; Fig. 13A</p>	<p>separate structures, unattached from one another, each adjacent a side edge of the optical cavity</p> <p><u>Intrinsic Support</u></p> <p>3:15-20; 3:42-67; 4:10-24; 7:3-31; 7:50-60; Figs. 3, 4, 11, 13.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT U**  
**CHI MEI USP 6,134,092**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
whereby light is injected from said exit mouths into a peripheral portion of said optical cavity	C	<p>not a claim limitation</p> <p>or</p> <p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>light is injected from regions of the optical cavities farthest from the point sources of light into a portion of the optical cavity that is covered by a cover</p> <p><u>Intrinsic Support</u></p> <p>3:18-22; 5:9-14; 6:66-7:26; 9:30-12:9; Fig. 3; Fig. 11; Fig. 12; Fig. 13; Fig. 13A</p>	<p>such that light is injected from said exit mouths into a boundary adjacent a side edge of the optical cavity</p> <p><u>Intrinsic Support</u></p> <p>1:43-52, 66-7; 3:18-22; 4:10-23; 5:9-15; 7:3-31, 26-30, 55-9; Figs. 5, 6A, 13, 13A.</p>

# **EXHIBIT V**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT V**  
**CHI MEI USP 6,734,926**

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
display apparatus	L	plain meaning  <u>Intrinsic Support</u>  Abstract, 1:7-11, 36-39, 2:17-3:24, 3:63-4:12, 4:50-5:21, 5:37-6:14, 6:28-50, 6:65-7:16, 7:24-33, 7:52-8:3, 8:28-33, Figs. 4-13	a display product, such as a monitor or television  <u>Intrinsic Support</u>  1:8-11, 36-53; 2:1-11; 8:4-27; Figs. 1, 3-13.
upper frame	L	plain meaning  <u>Intrinsic Support</u>  1:39-44, 2:17-24, 33-35, 51-54, 2:66-3:2, 4:1-3, 50-51, 5:1-3, 37-38, 55-58, 6:31-34, 8:28-33, Figs. 1, 4-13	the outermost front cover for the display product  <u>Intrinsic Support</u>  1:8-11, 36-53; 2:1-11; 8:4-27; Figs. 1, 3-13.
an array of light tubes disposed behind the display panel	L	plain meaning  <u>Intrinsic Support</u>  Abstract, 1:10-11, 45-53, 2:1-11, 17-22, 33-37, 51-55, 2:66-3:4, 4:1-5, 50-51, 5:1-5, 37-38, 55-59, 6:31-35, 8:28-33, Figs. 1, 4-13	multiple fluorescent lamps arranged along the back of the direct type backlight unit  <u>Intrinsic Support</u>  2:1-11; 3:18-24; 8:4-16; Figs. 4-13.

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT V**  
**CHI MEI USP 6,734,926**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
being separated from the side portion by a gap	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>there is a space between one side of a subframe of the supporting frame and the side portion of the reflecting plate</p> <p><u>Intrinsic Support</u></p> <p>2:24-32, 4:7-20, 50-62, 8:28-33, Figs. 4-5</p>	<p>positioned to form a space bounded by a sub-frame and a side portion</p> <p><u>Intrinsic Support</u></p> <p>4:35-39, 54-64; 5:15-21, 30-36, 40-51; 6:6-13, 49-51; 8:4-27; Figs. 4-7.</p>
a circuit board installed within the gap for controlling operations of the display apparatus	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>a rigid or printed circuit board for controlling certain operations of the display apparatus located in the space defined above</p> <p><u>Intrinsic Support</u></p> <p>2:24-32, 2:44-50, 4:7-20, 4:32-39, 50-62, 5:7-22, 30-33, 37-38, 41-51, 8:28-33, Figs. 4-7</p>	<p>a control circuit board is mounted in the space bounded by the sub-frame and the side portion and no control circuit board is located on the back of the supporting plate or reflecting plate</p> <p><u>Intrinsic Support</u></p> <p>1:7-11; 1:54-2:7; 3:18-24, 61-63; 5:19-21, 30-36; 6:25-27, 62-64; 8:4-27; Figs. 4-13; App 10/065,039, 1/26/01 Notice of Allowability, page 2.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT V**  
**CHI MEI USP 6,734,926**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
being separated from the side portion of the supporting plate by a gap	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>there is a space between one side of a subframe of the supporting frame and the side portion of the supporting plate</p> <p><u>Intrinsic Support</u></p> <p>2:44-50, 5:7-20, 37-38, 41-51, 8:28-33, Figs. 6-7</p>	<p>positioned to form a space bounded by a sub-frame and a side portion</p> <p><u>Intrinsic Support</u></p> <p>4:35-39, 54-64; 5:15-21, 30-34; 5:40-51; 6:6-13, 49-51; 8:4-27; Figs. 4-7.</p>
a circuit board installed on the side portion of the reflecting plate for controlling operations of the display apparatus	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>a rigid or printed circuit board for controlling certain operations of the display apparatus mechanically supported by the side portion of the reflecting plate</p> <p><u>Intrinsic Support</u></p> <p>2:58-65, 5:62-6:23, 8:28-33, Figs. 8-9</p>	<p>a control circuit board is mounted to the side of the reflecting plate and no control circuit board is located on the back of the supporting plate or reflecting plate</p> <p><u>Intrinsic Support</u></p> <p>1:7-11; 1:54-2:7; 3:18-24, 61-63; 6:25-27, 62-64; 8:4-27; Figs. 4-13; App 10/065,039, 1/26/01 Notice of Allowability, page 2.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT V**  
**CHI MEI USP 6,734,926**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
a circuit board installed on the side portion of the supporting plate for controlling operations of the display apparatus	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>a rigid or printed circuit board for controlling certain operations of the display apparatus mechanically supported by the side portion of the supporting plate</p> <p><u>Intrinsic Support</u></p> <p>3:3-17, 6:38-62, 8:28-33, Figs. 10-11</p>	<p>a control circuit board is mounted to the side of the supporting plate and no control circuit board is located on the back of the supporting plate or reflecting plate</p> <p><u>Intrinsic Support</u></p> <p>1:7-11; 1:54-2:7; 3:18-24, 61-3; 6:25-27, 62-64; 8:4-27; Figs. 4-13; App 10/065,039, 1/26/01 Notice of Allowability, page 2.</p>
integrated supporting unit	L	<p>a component including a supporting frame portion and either a reflecting plate portion or a supporting plate portion</p> <p><u>Intrinsic Support</u></p> <p>6:67-7:17, 7:27-43, 8:28-33, Figs. 12-13</p>	<p>a unitary structure that provides support</p> <p><u>Intrinsic Support</u></p> <p>4:5-20; 6:65-7:15; 7:26-40; Fig. 4.</p>
a circuit board installed on at least one of the side portions of the reflecting plate for controlling operations of the display apparatus		<p>a rigid or printed circuit board for controlling certain operations of the display apparatus mechanically supported by the side portion of the integrated supporting unit</p> <p><u>Intrinsic Support</u></p> <p>2:58-65, 5:62-6:23, 6:67-7:17, 8:28-33, Figs. 8-9, 12</p>	Indefinite

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT V**  
**CHI MEI USP 6,734,926**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
a circuit board installed on at least one of the side portions of the supporting plate for controlling operations of the display apparatus		a rigid or printed circuit board for controlling certain operations of the display apparatus mechanically supported by the side portion of the integrated supporting unit  <u>Intrinsic Support</u>  3:3-17, 6:38-62, 7:27-43, 8:28-33, Figs. 10-11	Indefinite

# **EXHIBIT W**

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT W**  
**CHI MEI USP 7,280,179**

**Disputed Constructions**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
forming a sealing member having a main portion enclosing a display region	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>forming sealing material in a closed shape having four side walls for fixing a pair of substrates to each other and sealing the liquid crystal layer in the display region</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:6-11; 1:17-39; 1:49-2:5; 2:17-28; 2:40-67; 3:7-15; 3:20-27; 3:45-54; 3:67-4:31; 4:34-37; 4:65-5:7; Figs. 1-4; App. 10/921,508, 4/26/06 Response, pages 8, 9, 10; 9/25/06 Amendment, pages 9, 10, 11, 12</p>	<p>depositing sealant material parallel to the edges of the display region so that it encloses the display region</p> <p><u>Intrinsic Support</u></p> <p>1:29-32, 49-52; 4:12-31; 5:3-7; Figs. 2, 3, and 4; App 10/921,508, 4/26/06 Response, pages 8-10, 12 and 13; App 10/921,508, 9/26/06 Response, pages 9-17; App 10/921,508, 3/1/07 Response, pages 10-16.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT W**  
**CHI MEI USP 7,280,179**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
the sealing member has a main portion enclosing a display region	L	<p>plain meaning</p> <p>or, if the Court determines that construction is necessary,</p> <p>sealing material in a closed shape having four side walls for fixing a pair of substrates to each other and sealing the liquid crystal layer in the display region</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:6-11; 1:17-39; 1:49-2:5; 2:17-28; 2:40-67; 3:7-15; 3:20-27; 3:45-54; 3:67-4:31; 4:34-37; 4:65-5:7; Figs. 1-4; App. 10/921,508, 4/26/06 Response, pages 8, 9, 10; 9/25/06 Amendment, pages 9, 10, 11, 12</p>	<p>the sealing member has a portion of sealant material that is parallel to the edges of and encloses the display region</p> <p><u>Intrinsic Support</u></p> <p>1:29-32, 49-52; 4:12-31; 5:3-7; Figs. 2, 3, and 4; App 10/921,508, 4/26/06 Response, pages 8-10, 12 and 13; App 10/921,508, 9/26/06 Response, pages 9-17; App 10/921,508, 3/1/07 Response, pages 10-16.</p>
overlapping area extends along one side of the display region	L	<p>plain meaning</p> <p><u>Intrinsic Support</u></p> <p>1:52-56; 2:56-67; 3:7-15; 4:18-31; 4:65-5:7; Figs. 1-4</p>	<p>a segment of the sealing member main portion where sealant material is applied on top of previously applied sealant material along one edge of the display region</p> <p><u>Intrinsic Support</u></p> <p>1:52-61; 4:12-31; Figs. 2, 3, and 4; App 10/921,508, 3/1/07 Response, pages 10-16; App 10/921,508, 6/5/07 Reasons for Allowability, page 2.</p>

**JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT W**  
**CHI MEI USP 7,280,179**

<b>Claim Terms</b>	<b>Des.</b>	<b>CMO Construction</b>	<b>LGD Construction</b>
applying the sealing material along the display region to form the main portion of the sealing member	L	<p>Plain and ordinary meaning in light of previous constructions.</p> <p><u>Intrinsic Support</u></p> <p>Abstract; 1:6-11; 1:17-39; 1:49-2:5; 2:17-28; 2:40-67; 3:7-15; 3:20-27; 3:45-54; 3:67-4:31; 4:34-37; 4:65-5:7; Figs. 1-4; App. 10/921,508, 4/26/06 Response, pages 8, 9, 10; 9/25/06 Amendment, pages 9, 10, 11, 12</p>	<p>depositing sealant material parallel to the edges of the display region</p> <p><u>Intrinsic Support</u></p> <p>1:29-32, 49-52; 4:1-31; 5:3-7; Figs. 2, 3, and 4; App 10/921,508, 4/26/06 Response, pages 8-10, 12 and 13; App 10/921,508, 9/26/06 Response, pages 9-17; App 10/921,508, 3/1/07 Response, pages 10-16.</p>